

# IMPROVEMENT IN PERFORMANCE OF CASCADED MULTILEVEL INVERTER USING TRIANGULAR AND TRAPEZOIDAL TRIANGULAR MULTI CARRIER SVPWM

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DOI: 10.15598/aeec.v14i5.1767

**Abstract.** In this paper a new Trapezoidal Triangular Multi Carrier SVPWM (TTMC-SVPWM) technique has been proposed for a cascaded H bridge multilevel inverter. This technique has been implemented for a 11-level cascaded H-bridge multilevel inverter to evaluate the performance parameters and also to compare it with other types of carrier based PWM techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and Phase Shifted Carrier (PSC) PWM techniques. The simulation has been carried out for 11-level H-bridge multilevel inverter using MATLAB/Simulink. The detailed analysis of the results has been presented and studied in terms of fundamental component of output voltage and THD.

## Keywords

*APODSVPWM, cascaded H-bridge, multi-level inverter, PODSVPWM, PSCSVPWM, TTMC-PDSVPWM.*

## 1. Introduction

In recent years much work has been carried out on Multilevel Inverters (MLI) to reduce harmonics in the output current and voltage waveforms. These harmonics result in extra power loss. All undesired operating characteristics exhibited by converters can be overcome in multi-level converters using a proper PWM technique. Multilevel inverters are used more popularly for

generating higher voltage levels with reduced harmonics. This topic has been discussed in detail in [1], [2], [3], [4] and [5]. Each converter of MLI operates at a low switching frequency, thus reducing the stress on semiconductor devices, and the power loss due to switching is reduced [6] and [7]. Increase in number of levels in the inverter stage leads to the generation of staircase voltage waveform, which has a reduced harmonic distortion. On the other side higher number of levels increase the complexity in inverter control and present voltage inequality problems. Multilevel inverters are found to be suitable for static VAR compensators, active power filters and motor drive applications. Common mode voltages are the major issues in the MLI when they are interfaced with drives and they can be overcome with sophisticated modulation methods [8].

Multilevel inverters are classified into [9]:

- diode clamped or neutral point clamped,
- capacitor clamped or flying capacitor,
- cascaded multilevel inverters.

Due to modularity and simplicity in control Cascaded H-Bridge (CHB) MLI are used broadly in practical applications. Number of output phase voltage levels in cascaded inverter are  $2n + 1$ , where  $n$  is the number of H bridges used in one phase.

Several SPWM techniques like PDSPWM, PODSPWM and APODSPWM techniques have already been implemented on MLI. These techniques have high THD and low magnitude in output voltage. These can be improved by using the proposed techniques.

In this paper various carrier pulse width modulation methods are introduced and compared. In addition to this a new modulation method named Trapezoidal Triangular Multi Carrier (TTMC) SVPWM is introduced and implemented and compared with other methods. This modulation method gives higher output voltage and better harmonic distortion.

## 2. Multi Carrier SPWM Techniques

By implementing modulation technique, low frequency voltage harmonics are removed perfectly. This modulation technique produces nearly perfect sinusoidal waveforms, with lower THD. A very wide spread method in industrial applications is the classic carrier-based Sinusoidal PWM (SPWM) that uses the carrier shifting technique to condense the harmonics in voltages generated by inverters. The carriers used in multilevel inverter may be shifted vertically or horizontally.

The vertically shifted carrier scheme can be easily realizable on any digital controller. This scheme comes with three different techniques:

- All carrier signals are in Phase (Phase Disposition (PD)).
- Half of the carrier signals above are in same phase and half below carriers are in same phase but the phase difference between these two half's is  $180^\circ$  (Phase Opposition Disposition (POD)).
- All carriers are alternately in opposition (Alternate Phase Opposition Disposition (APOD)).

If the carriers are shifted horizontally corresponding PWM is Phase Shifted Carrier PWM (PSCPWM). The number of carriers required are  $(m - 1)$  for an  $m$  level inverter in all the variants.

In the APOD, the sideband harmonics corresponding to first set are centered around the carrier frequency. In the APOD and the POD, harmonics will not exist at pulse number  $m_f$ , due to odd symmetry of their PWM waveforms. The APOD and the POD strategies provide similar performance for three level converters [10]. In PD, the triplen harmonics of voltage will be removed because the waveforms are asymmetric and thus harmonics at  $m_f$  are removed if  $m_f$  is chosen as a multiple of three. So the PD is more expedient due to minute values of other harmonics. The PD strategy is now well recognised for attaining the lowest line-to-line harmonic voltage distortion.

The PSCSVPWM technique results in the termination of all carrier and connected sideband harmonics

up to  $2N_c^{th}$  carrier group, where  $N_c$  is the number of H-bridges in each phase. Phase Shifted Carrier PWM (PSCPWM) is the common PWM for cascaded MLI. The switching transitions for PSCPWM are  $2N$  times the number of switching transitions for APOD.

### 2.1. Modulation Index

The modulation index is the ratio of peak magnitudes of the modulating signal  $V_m$  and the carrier signal  $V_c$ .

$$m = \frac{V_m}{V_c} \quad (1)$$

The modulation index in SPWM technique for cascaded multilevel inverter configuration is given by:

$$m = \frac{V_m}{(N - 1)V_c}, \quad (2)$$

where  $N$  is number of levels. For undermodulation  $0 < m < 1$ . For overmodulation  $m > 1$ .

Generally, overmodulation is not desired because of the presence of the lower frequency harmonics in the output voltage and subsequent distortion in the load current.

### 2.2. Frequency Modulation Ratio or Pulse Number ( $m_f$ )

It is the ratio of frequency of the triangular carrier signal  $f_c$  to the frequency of sinusoidal reference signal  $f_s$ . It controls harmonics in the output voltage.

$$m_f = \frac{f_c}{f_s} \quad (3)$$

#### 1) For an Odd Integer Value of $m_f$ :

To reduce the harmonics in output voltage, carrier signal would be synchronized with the reference signal. The carrier signal frequency  $f_c$  is an integer multiple of the reference sinusoidal signal frequency  $f_s$ , that is the pulse number  $m_f$  must be an exact integer. Sub harmonics will exist at the inverter output voltage, if  $m_f$  is not an integer [11]. The output voltage signal generated by implementing of SPWM technique has harmonics of several orders in the phase voltage waveform. The leading harmonics are of fundamental and other order of  $m_f$  and  $m_f \pm 2$ . Thus  $m_f$  would be an odd integer to diminish even harmonics. If  $m_f$  is not odd, DC component may exist and even harmonics will be present at output voltage [11].

### 2) For $m_f$ as a Multiple of 3:

The triplen harmonics of three-phase PWM inverter will be reduced by selecting  $m_f$  as multiple of 3. Selecting a multiple of 3 is also expedient to use the same triangular waveform as the carrier in all three phases, leading to some simplification in hardware control and implementation [12].

### 3) For High $m_f$ :

The PWM technique pushes the harmonics into the high frequency range nearby the carrier frequency and its multiples. Harmonic content at inverter output is reduced with larger number of pulses that is with high value of  $m_f$  or  $f_c$ . But, a high carrier frequency results in larger number of switchings per cycle and therefore the power loss increases.

In few circumstances the ratio of carrier signal frequencies and modulating signal frequencies cannot be very high but the pole voltage has a fundamental frequency component in-phase and proportionate to the modulating signal. The vital benefit of having very high carrier frequency, in contrast to the modulating wave frequency, is that the useful fundamental frequency component of pole voltage and unwanted harmonics are far apart on the frequency spectrum. We can virtually filter away the harmonic voltages without attenuating the magnitude of the fundamental frequency component by choosing a proper low pass filter. If the harmonics are of high frequencies, then the required filter size is to be small.

In AC motor drive application, the intrinsic low pass filtering characteristics of the motor load are enough to reasonably block the harmonic current flow to the load. In such cases requirement of filter may not arise. The switches used in high power applications can be switched on only at sub kilohertz frequency and hence the carrier frequency will not be high. The switching frequency losses should also be considered before deciding the carrier frequency of the sine-PWM inverter. The switching frequencies in this case are 1050 Hz ( $m_f = 21$ ) and 1350 Hz ( $m_f = 27$ ).

Quarter and half wave symmetry safeguards that even harmonics will not exist in the output voltage spectrum. This can be realised by choosing  $m_f$  odd. Significant even harmonic which is removed, is the DC component. The harmonic components below the fundamental frequency known as sub-harmonics will not exist. For different power system applications, the switching frequencies typically range from 2 kHz to 15 kHz [11].

## 3. Generalized TTMC - Space Vector PWM for Cascaded Multilevel Inverter

In conventional SVPWM for multilevel inverters to find the switching time duration, for different inverter vectors, the mapping of the outer sectors to an inner sub hexagon sector is to be done. The switching inverter vectors corresponding to the concrete sectors are switched and the time periods premeditated from the mapped inner sectors. Implementing such a scheme in multilevel inverters will be very difficult, because higher number of sectors and inverter vectors are present. And in this method the computation time is increased for real time application.

In carrier based PWM scheme a proper offset voltage is added to sinusoidal references before comparing with carrier waves, to attain the performance of a SVPWM [13]. The offset voltage calculation is based on the modulus function depending on the DC link voltage, the number of levels and the phase voltage amplitudes.

One more modulation scheme is offered where sinusoidal reference phase voltages are added with common mode voltage of suitable magnitude all through the duration [14] and [15]. Addition of common mode voltage will not give SVPWM like performance, because middle inverter vectors will not be centered in a sampling interval [16]. Another modulation technique is offered in [17], where a fixed common mode voltage is added to the reference phase voltage all through the modulation range.

A simplified method is presented, where correct offset times are determined for centering the time durations of middle inverter vectors in a sampling interval. A procedure is given in [18] and [19] for finding the maximum probable peak amplitude of the fundamental phase voltage in linear modulation. The following equations are used to calculate offset time  $T_{offset}$ .

$$T_a = \frac{V_a \cdot T_s}{V_{dc}}, \quad (4)$$

$$T_b = \frac{V_b \cdot T_s}{V_{dc}}, \quad (5)$$

$$T_c = \frac{V_c \cdot T_s}{V_{dc}}, \quad (6)$$

where  $T_a$ ,  $T_b$  and  $T_c$  are the time periods of imaginary switching, proportional to the instantaneous values of the reference phase voltages  $V_a$ ,  $V_b$  and  $V_c$ .  $T_s$  is the sampling time period.

$$T_{offset} = \frac{T_0}{2} - T_{min}, \quad (7)$$

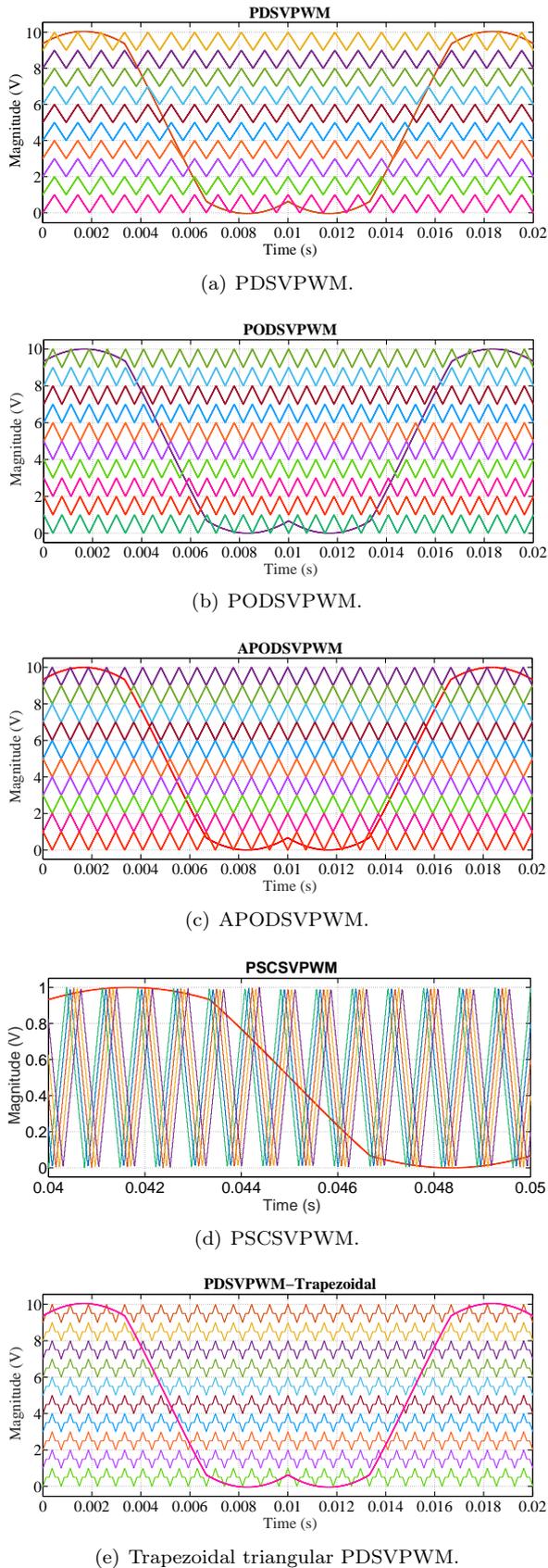


Fig. 1: Different modulation techniques.

$$T_0 = T_s - T_{effect}, \tag{8}$$

$$T_{effect} = T_{max} - T_{min}, \tag{9}$$

where  $T_{max}$  is the maximum magnitude of the three reference phase voltages, in a sampling interval and  $T_{min}$  is the minimum magnitude of the three reference phase voltages, in a sampling interval.

The inverter switching vectors are centered in a sampling interval by the addition of offset voltage to the reference phase voltages that equates the performance of SPWM technique with the SVPWM technique [20]. Figure 1 shows the different modulation techniques by the comparison of modulating wave generated in generalized SVPWM with triangular wave and trapezoidal triangular wave.

This proposed SVPWM signal generation does not involve look up table, sector identification, angle information and voltage space vector amplitude measurement for switching vector determination required in the conventional multilevel SVPWM technique. This scheme is more effective when compared with conventional multilevel SVPWM technique.

### 4. Simulation Results and Discussion

Simulations are carried out using Matlab/Simulink environment for 11-level cascaded H-bridge MLI by implementing proposed TTMC-SVPWM and TTMC-SPWM techniques. A 3 phase induction motor is con-

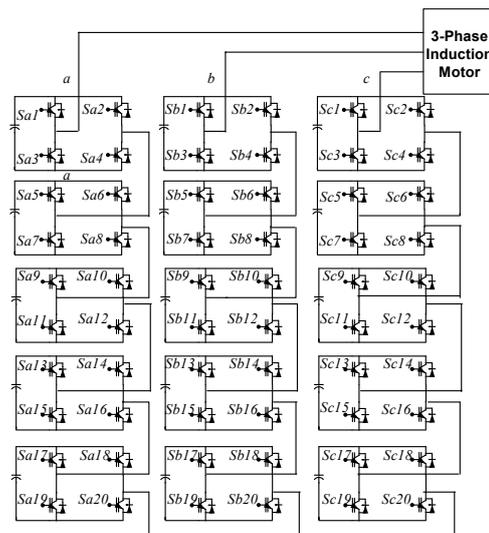


Fig. 2: 11-level cascaded H-bridge multilevel inverter.

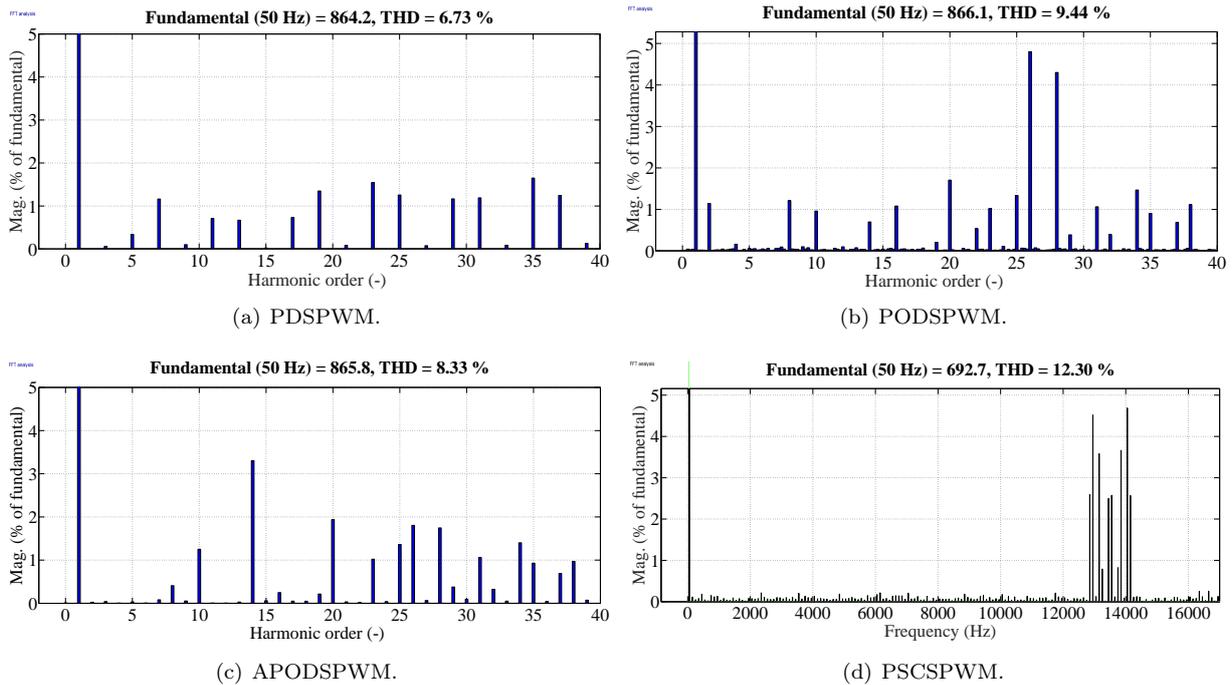


Fig. 3: Harmonic analysis for different SPWM Techniques with triangular carrier and  $m_f = 27$ .

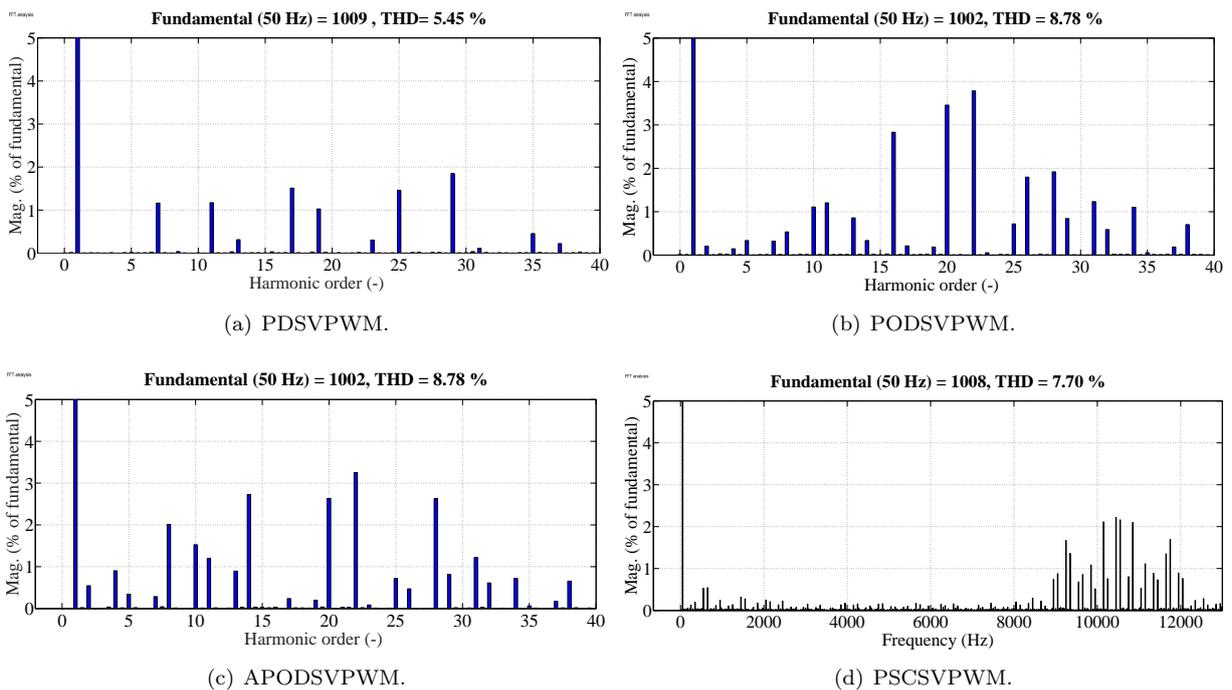


Fig. 4: Harmonic analysis for different SVPWM techniques with triangular carrier and  $m_f = 21$ .

considered as load for this scheme. The separate DC voltage sources are set to 100 V for each H-bridge and the switching frequencies are 1050 Hz and 1350 Hz considered for triangular and trapezoidal triangular carrier waves. The simulated 11-level cascaded H-bridge MLI connected to induction motor load is shown in Fig. 2.

Each phase consists of five H-bridges to generate 11-levels in phase voltage.

Figure 3 shows the harmonic analysis of inverter output line voltage for different SPWM techniques with triangular carrier having  $m_f$  of 27. The fundamental component magnitude in PDSVPWM, PODSVPWM

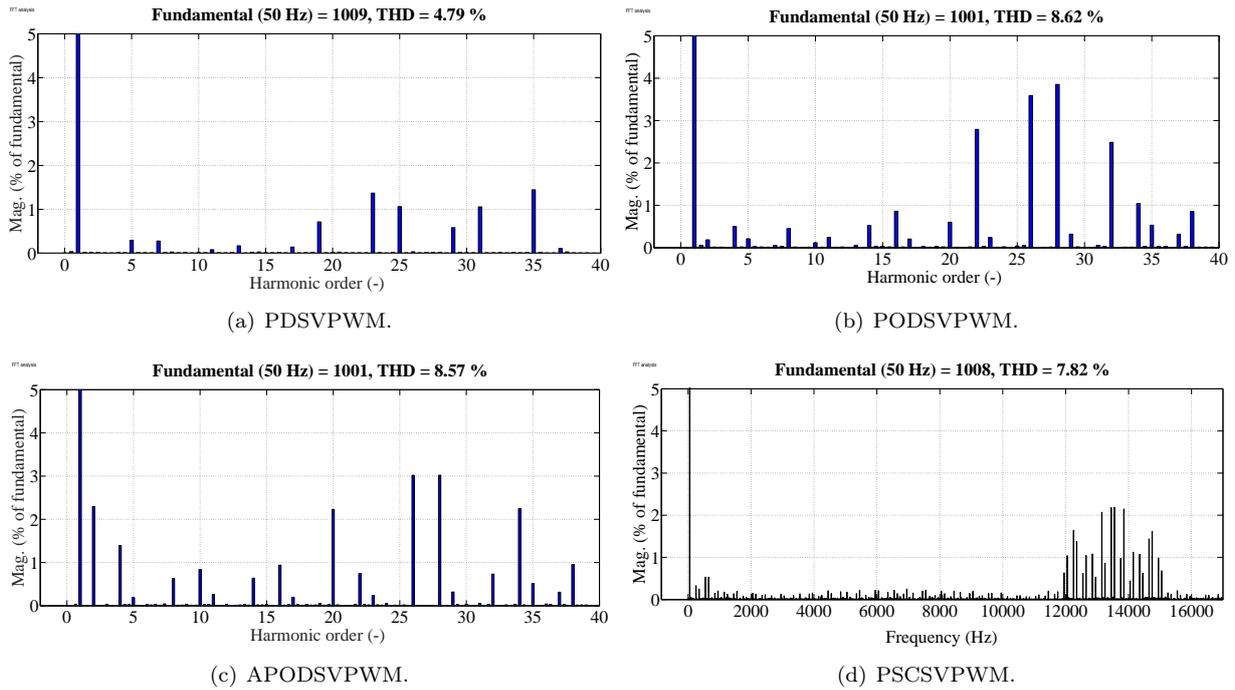


Fig. 5: Harmonic analysis for different SVPWM techniques with triangular carrier and  $m_f = 27$ .

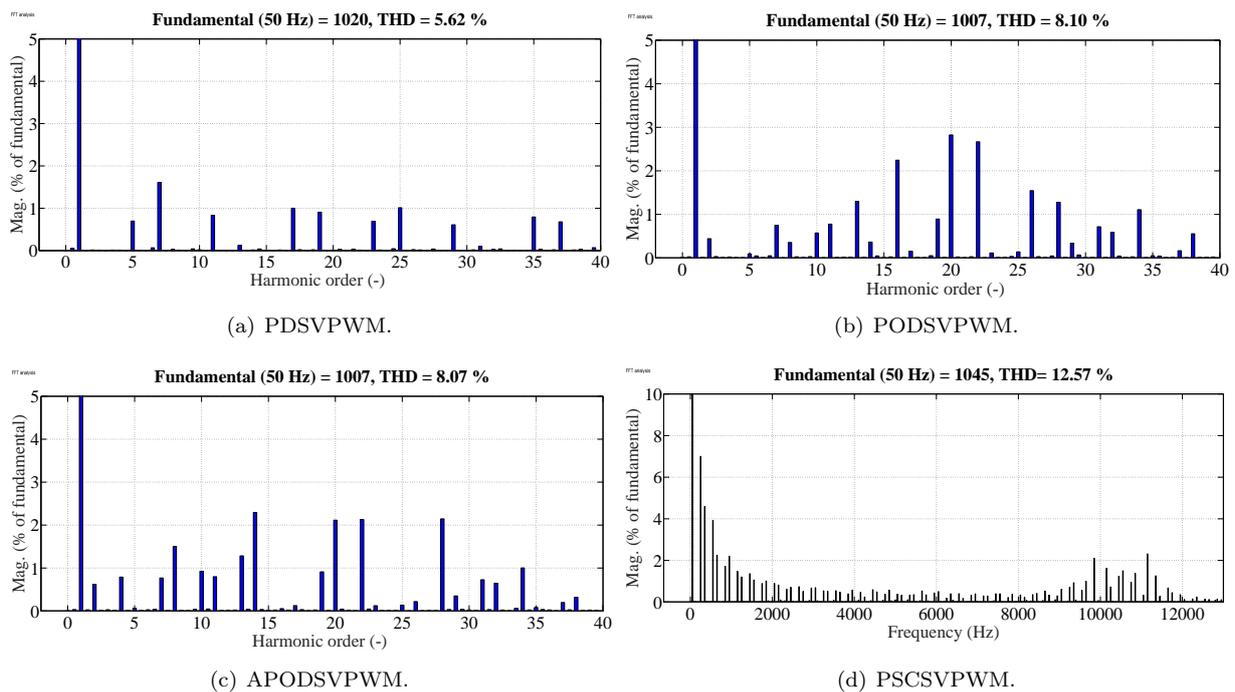


Fig. 6: Harmonic analysis for different SVPWM techniques with trapezoidal carrier and  $m_f = 21$ .

and APODSVPWM is the same and it is more than PSCPWM technique. In PSCPWM technique no harmonics present up to  $2N_c^{th}$  carrier group that is up to 13.5 kHz for carrier frequency of 1350 Hz. The PDSVPWM technique gives better harmonic performance in comparison to the other SPWM techniques.

Figure 4 and Fig. 5 show the harmonic analysis of inverter output line voltage for different SVPWM techniques with the triangular carrier wave having  $m_f$  of 21 and 27. The fundamental component of output voltage in all the PWM techniques is almost the same but 15 % more than all the SPWM techniques except PSCPWM. The performance of PODSVPWM

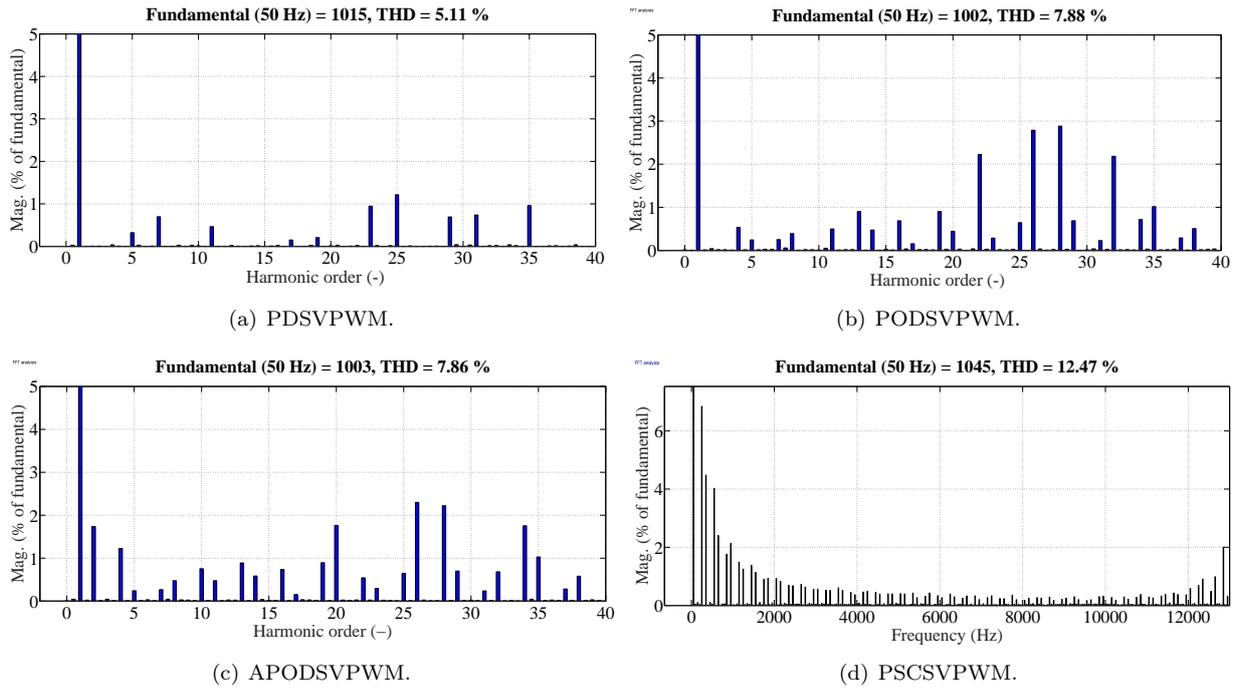


Fig. 7: Harmonic analysis for different SVPWM techniques with trapezoidal carrier and  $m_f = 27$ .

and APODSVPWM techniques is almost the same in terms of THD, but PSCSVPWM performance is better than the performance of these two methods. The PDSVPWM technique gives 5.45 % of THD, which gives better performance with respect to all other techniques. If the carrier frequency increases, the THD in PDSVPWM, PODSVPWM and APODSVPWM techniques reduces, whereas no change is observed in the magnitude of fundamental component. In PSCPWM technique the harmonics are shifted towards higher frequency.

Figure 6 and Fig. 7 show the harmonic analysis of output line voltages, when the inverter is controlled by different SVPWM techniques with trapezoidal triangular carrier waves having  $m_f = 21$  and  $m_f = 27$ . In this SVPWM technique with  $m_f = 21$ , the magnitude of fundamental component is increased in all techniques but the THD is almost the same as triangular carrier wave except the PSCSVPWM. In PSCSVPWM the THD values are increased corresponding to the triangular carrier wave. If the carrier frequency is increased, there is a reduction in the THD in all the methods except PSCSVPWM. The performance of PSCSVPWM remains the same even though carrier frequency increased.

Table 1 shows the comparison of different SPWM techniques with trapezoidal triangular carrier and different SVPWM techniques with triangular carrier and trapezoidal triangular carrier waves. It is observed from tabulated simulation results that PDSVPWM technique with triangular carrier wave having  $m_f$  of

Tab. 1: Comparison of %THD and fundamental component of voltage for different PWM techniques.

S. no.	PWM technique	Fundamental component of line voltage	THD (%)
<b>SPWM-triangular carrier wave with <math>\{m_f = 27\}</math></b>			
1	PDSPWM	864.2	6.73
2	PODSPWM	866.1	9.44
3	APODSPWM	865.8	8.33
4	PSCSPWM	692.7	12.30
<b>SVPWM-triangular carrier wave with <math>\{m_f = 21\}</math></b>			
5	PDSVPWM	1009	5.45
6	PODSVPWM	1002	8.78
7	APODSVPWM	1002	8.78
8	PSCSVPWM	1008	7.70
<b>SVPWM-triangular carrier wave with <math>\{m_f = 27\}</math></b>			
9	PDSVPWM	1009	4.79
10	PODSVPWM	1001	8.62
11	APODSVPWM	1001	8.57
12	PSCSVPWM	1008	7.82
<b>SVPWM-trapezoidal triangular carrier wave with <math>\{m_f = 21\}</math></b>			
13	PDSVPWM	1020	5.62
14	PODSVPWM	1007	8.10
15	APODSVPWM	1007	8.07
16	PSCSVPWM	1045	12.57
<b>SVPWM-trapezoidal triangular carrier wave with <math>\{m_f = 27\}</math></b>			
17	PDSVPWM	1015	5.11
18	PODSVPWM	1002	7.88
19	APODSVPWM	1003	7.86
20	PSCSVPWM	1045	12.47

27 gives better THD as 4.79 % and 1009 V fundamental voltage. Whereas the PDSVPWM technique with trapezoidal triangular carrier wave having  $m_f$  of 21 gives better THD of 5.11 % and 1020 V fundamental component of voltage.

## 5. Conclusion

In this paper new trapezoidal triangular multicarrier SVPWM techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD), and Phase Shifted Carrier PWM (PSCPWM) have been implemented for 11-level cascaded MLI. The above results are compared among each other and with different trapezoidal triangular carrier SPWM techniques. It is observed that PDSVPWM technique with 1350 Hz triangular carrier wave gives 4.79 % of THD, which is the better performance for a 11 cascaded H-bridge MLI, whereas PDSVPWM with 1350 Hz trapezoidal triangular carrier gives 1015 voltage of high fundamental component and 5.11 % of THD value. It is concluded that triangular carrier PDSVPWM gives better THD, with trapezoidal triangular carrier wave, all the techniques give high fundamental component of line voltage, but PSCPWM with trapezoidal triangular carrier wave gives higher fundamental component voltage among all other techniques along with higher THD values. In all these methods if the carrier frequency is increased beyond 1350 Hz, the THD in the line voltage is increased.

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