Dynamic Power Consumption and Delay Analysis for Ultra-Low Power 2 to 1 Multiplexer Designs

Nishant KUMAR[1], *Poornima MITTAL*[1], *Bhawna RAWAT*[1], *Mudit MITTAL*[2]

[1]Department of Electronics and Communication Engineering, Delhi Technological University, Main Bawana Road, 110042 Delhi, India
[2]Department of Information Technology, Institute of Technology and Management, 60 Chakarata Road, 248001 Dehradun, India

nishant205kumar@gmail.com, poornimamittal@dtu.ac.in, bhawnarawat12@gmail.com, mushi172@gmail.com

DOI: 10.15598/aeee.v19i2.3821

Article history: Received May 23, 2020; Revised Apr 03, 2021; Accepted Apr 04, 2021; Published Jun 30, 2021.

Abstract. *This paper highlights a comparative analysis of eight diverse techniques for 2 to 1 multiplexer implementation. The functionality is identical but significant differences in dynamic power consumption and propagation delay are observed. This paper aims to enable the designer to pick out the best fit structure for a specific application in keeping with their design requirement. The multiplexers are designed at 90 nm technology node and simulated at a supply voltage of 1 V.*

Keywords

Average power dissipation, CMOS, dynamic power, leakage power, low power application, power delay product, standard cells.

1. Introduction

Technology is pacing at an exponential rate against time. Devices are being remodelled and improved within short spans to outdo themselves. Consequently, each component of a device is being analysed to improve its performance. Designers are ceaselessly trying to improve the performance of the existing devices or trying to devise a new way to design and improve the performance [1]. A multiplexer is one of the basic building blocks of digital systems [2] and [3]. In this paper, different design techniques of 2 to 1 multiplexer are compared.

The advancements in design automation of ASICs have enabled positioning millions of transistors on a single chip for robust circuitry implementation. Consequently, the density of transistors for a given area has increased significantly, thereby leading to an increase in formidable designing issues [4]. Henceforth, the solutions that have been recommended suggest a reduction of the transistor power supply voltage, switching frequency, and capacitance [5], [6] and [7]. Depending on the application, different types of circuits and design methodologies were proposed which disallowed the formulation of uniform rules for optimum logic types.

The smallest multiplexer that can be designed is a 2 to 1 multiplexer. It forms the building block for other larger multiplexer modules [8] and optimising its configuration enhances its stability [9]. Therefore, to optimise the performance of 2 to 1 multiplexer, different configurations including Gate Diffusion Input (GDI), Pass Transistor (PT), Multiplexer Single with Level Restoration (MSL), Transmission Gate (TG), Static CMOS, Complementary Pass Logic (CPL), Cascode Voltage Switch Logic (CVSL) and Multi Threshold CMOS CVSL (MTCMOS CVSL) are analysed in this paper. All the multiplexers are designed using complementary MOSFET transistors at 90 nm technology node. Further, their performance is analysed and compared by means of output response and dynamic power dissipation using Cadence Virtuoso software. Additionally, power and delay are analysed to find the best multiplexer amongst all the configurations.

This paper is arranged into five sections, including this introductory section. Further, Sec. 2. illustrates schematics diversity and working for different multi-

plexer configurations. The output response for different multiplexer designs is presented and discussed in Sec. 3. . Additionally, dynamic power dissipation and delay response are elaborated in Sec. 4. . Finally, evaluated structures' properties are summarized in Sec. 5. .

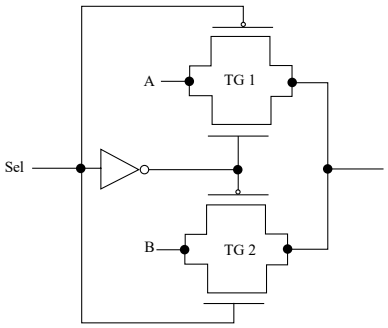
2. CMOS Structures of Multiplexers

Diverse structures of 2 to 1 multiplexer are simulated and analysed. Designs such as GDI and PT multiplexer have simpler schematic and utilize lesser area with low power dissipation but with degraded output response. Other techniques such as MSL, Static CMOS, CPL, CVSL and MTCMOS based multiplexer are liable for producing non-degraded output but consume more power and introduce larger delay, as well.

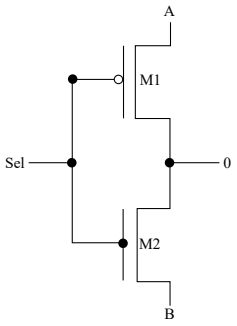
Transmission gate based 2 to 1 multiplexer is designed using a pair of Transmission Gates (TGs). Each TG is a pair of NMOS and PMOS transistors wherein the source and drain terminals of transistors are connected in parallel, as illustrated in Fig. 1(a). Both NMOS and PMOS permit the same input simultaneously. Thus, it is transferred to the output node through this TG without any deterioration [10]. At high input signal, the NMOS gives a weak 1 at the output. However, PMOS provides a strong 1 at the same time, thereby maintaining the output level. Similarly, at low input, the PMOS produces a weak 0 but NMOS supplies a strong 0 at the output [11]. TG configuration is used to isolate the components and signals/data from being transmitted to the other nodes without using any other hardware.

Gate Diffusion Input (GDI) logic allows the user to design complex logic circuits using a smaller number of transistors. The basic structure of GDI resembles a CMOS inverter and inherits characteristics of CMOS and PTL logic [12]. This is an appropriate technique for designing fast and low-power circuits using fewer transistors as compared to CMOS and PTL techniques [13] and [14]. The schematic for the GDI based 2 to 1 multiplexer is given in Fig. 1(b). When Sel = 1, the NMOS transistor operates in ON mode and input signal B will pass to the output; O. On the other side, output O receives the input signal A, when Sel is maintained at 0.

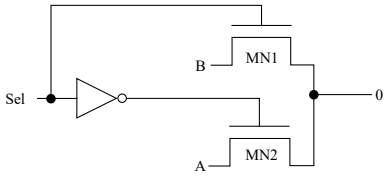
The GDI based multiplexer employs A and B inputs to the multiplexer, while the Sel signal acts as the select line and determines the input that gets transmitted to the output. The logical function implemented by the GDI based SRAM bit cell is nSel.A+ Sel.B. The advantages associated with the GDI technique are minimal transistor requirements, low power dissipation and fast operation. However, the limitations of this structure encounters are - (1) If A = 0, then PMOS being a weak 0 will not pass a perfect 0 at the output, (2) The complementary is applicable for B = 1, as NMOS delivers weak 1 to output.



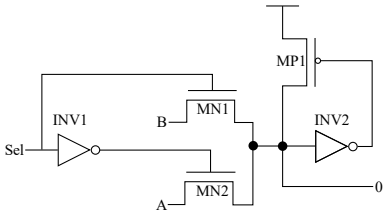
(a) TG based multiplexer.



(b) GDI based multiplexer.



(c) PT based multiplexer.



(d) MSL based multiplexer.

Fig. 1: Schematic of TG, GDI, PT, and MSL based multiplexers.

Pass Transistor Logic (PTL) uses two NMOS transistors in pass transistor configuration. This logic is different from CMOS design as the source side of the logic network is connected to the input signal instead of the power supply [15], [16], [17] and [18], as depicted in Fig. 1(c). When Sel = 0, the MN2 transistor is saturated that leads the value at A to appear at the output terminal. Whereas, for Sel = 1, the value at B gets transferred to the output. The upsides

of PTL are high speed, low power consumption and low interconnect effect. However, the factor that limits the use of PTL technique is reduced signal integrity due to the inability of NMOS to pass a strong 1 [19]. Therefore, at conditions such as Sel = 1, B = 1 or Sel = 0, A = 1, the output driving capabilities are weak.

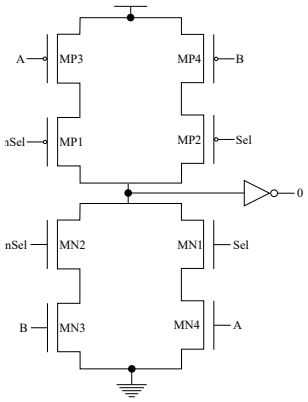
The shortcoming of the PT based multiplexer is modified and MSL based multiplexer is created. In this design, an additional PMOS transistor is used to restore the output level. The gate of the PMOS (MP1) is driven by an inverter (INV1) controlled by the output of the PT based multiplexer [20]. The gate and drain of PMOS (MP1) are connected to the output and input of the second inverter (INV2), respectively, as indicated in Fig. 1(d). Similarly, gate terminals of both NMOS transistors (MN1 and MN2) are connected to the input and the output of the first inverter (INV1). The purpose of designing MSL based multiplexer is to overcome the drawback of output deterioration and complex synthesis methodology for PT multiplexer [21]. When Sel = 1 and B = 1, NMOS produces a weak 1 as explained in the previous subsection. To rectify it, MSL based multiplexer converts this 1 to 0 through the inverter [22]. This inverter then drives the PMOS to ON state, thereby making the output signal a strong 1. The other advantage of MSL based multiplexer is maximum output swing (nearly V_{DD} and 0).

The next multiplexer implementation for analysis is Static CMOS based multiplexer. This multiplexer uses eight transistors, wherein four PMOS transistors form the pull-up network and the other four NMOS transistors form the pull-down network. This multiplexer utilizes inverted inputs and delivers inverted output; OB along with the actual output; O. The schematic for static CMOS based multiplexer is illustrated in Fig. 2(a) [23]. When Sel = 0, B = 0 or nSel = 1, A = 1/0, the MP2, MP4, MN2 are ON and MN1, MN3, MP1 are OFF, thus output becomes 0. There is some leakage due to MN2 and MN4 of the pull-down network. Similar observations are achieved for nSel = B = 1 or Sel = 0, A = 0/1 and 1 is produced at the output O. With similar phenomena, a zero output is produced for nSel = A = 0 or Sel = 1, B = 0/1. In such a condition, the leakage occurs through MN2 and MN4 of the pull-down network. This analysis concludes that the input B/A gets produced at the output for Sel = 0/1.

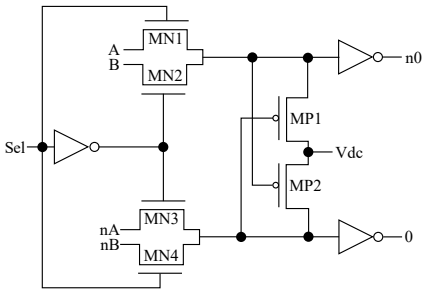
Complimentary Pass Transistor Logic (CPL) comprises three inverters and six transistors of which four are NMOS transistors and two are PMOS transistors. The NMOS transistors (MN1, MN2, MN3, and MN4) are connected in pairs as pass transistors. A pair of NMOS (MN1-MN2) is used to pass the input signal, while the other pair (MN3-MN4) is used to provide inverted input. The PMOS pair (MP1-MP2) is used for level restoration. The inverters are used to invert the select signal and the output. In this circuit, half of the transistors are used to pull up, while the other half is used to pull down the logic, thereby providing both actual output (O) and its complement (nO), as depicted in Fig. 2(b). When Sel = 0, transistors MN2-MN3 are turned ON and pass input signal B and nB (complement of input B) to O and nO, respectively. If input B = 0 (i.e. nB = 1), MP2 is ON. Therefore, V_{DC} gets connected to the output of MN3 and restores the logic level 1. Hence, 0 is produced at the output of the inverter. Now, if B = 1 (nB = 0), transistor MP1 is ON, the V_{DD} gets connected to the output of MN2 and logic level 1 is restored. Accordingly, inverted output (nO) is 0. This technique exhibits advantages like the presence of both output and inverted output, fast operation and restoration of output level. But this structure dissipates significantly more power than other structures, thereby limiting its application.

Cascode Voltage Switch Logic (CVSL) multiplexer is shown in Fig. 2(c). The NMOS logic forms the pull-down network and generates the complementary logic. CVSL is composed of a differential latching circuit and a cascaded complementary logic array [24]. Therefore, this structure is also acknowledged as Differential Cascode Voltage Switch Logic (DCVS or DCVSL) [20] and [23]. When Sel = 0, A = 0, transistors MN3, MN5, and MN6 are ON, henceforth, the output and gate of MP2 get connected to the ground terminal through transistor MN5 and MN6. Thus, the output obtained at O = 0 (nO = 1). For Sel = 0, A = 1, transistors MN3, MN4, and MN5 are ON and the ground gets connected to the output O through MN3 and MN4, thereby making the output nO = 0 and O = 1 as it gets connected to V_{DC} owing to the ON state of MP1. This configuration exhibits an advantage of reduction in number of PMOS transistors from each logic function leading to a significant area reduction.

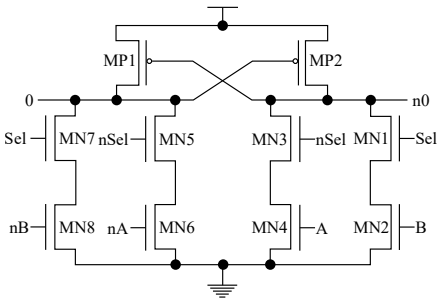
The functionality of Multi-Threshold CMOS Cascode Voltage Switch Logic (MTCMOS CVSL) based multiplexer is similar to the CVSL multiplexer. This technique is used to reduce the circuit leakage in static conditions [24]. In this configuration, one pair of PMOS-NMOS (MP3-MN9) is used, wherein MP3 isolates the logic circuit from V_{DC} and MN9 isolates the ground, as shown in Fig. 2(d). MTCMOS technique separates the circuit from the power supply and ground to prevent power dissipation in static state [25]. Here, two complemented sleep signals; Sleep and nSleep (complement of sleep signal) are used to control the gates of PMOS (MP3) and NMOS (MN9), respectively. When sleep is low, the circuit works as standard CVSL based multiplexer. During sleep state, both outputs are in High Z (high impedance) state and the circuit is non-operational.



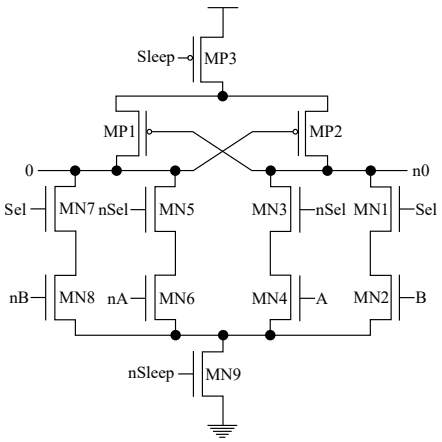
(a) Static CMOS based multiplexer.



(b) CPL based multiplexer.



(c) CVSL based multiplexer.



(d) MTCMOS CVSL based multiplexer.

Fig. 2: Schematic of static CMOS, CPL, CVSL, and MTCMOS CVSL based multiplexers.

3. Output Response and Analysis

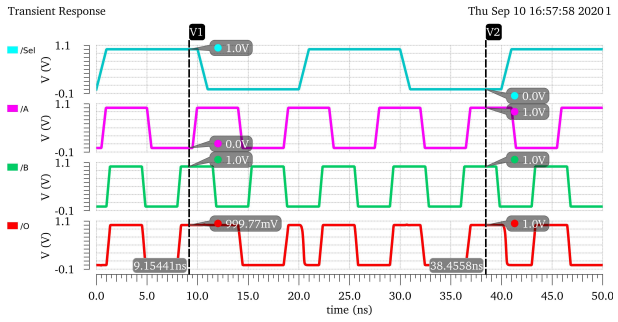
In this section, the output responses corresponding to different multiplexer structures discussed in the previous section are analyzed. The rise and fall timing values for A, B and Sel are incorporated as 0.45 ns, 0.35 ns and 1 ns, respectively. To analyze the realistic performance of multiplexers, a load capacitor of 1 fF [26] is used at the output.

In an ideal scenario, the generated output waveform will attain 0 V and 1 V level as per the input combination and select line configuration. If the output waveform is unable to attain a perfect 0 V or 1 V level, it is a non-ideal waveform. The output waveforms generated for all multiplexer structures discussed are ideal except for GDI, PT and MTCMOS CVSL. The output waveforms for ideal and non-ideal response for different multiplexer techniques are illustrated in Fig. 3.

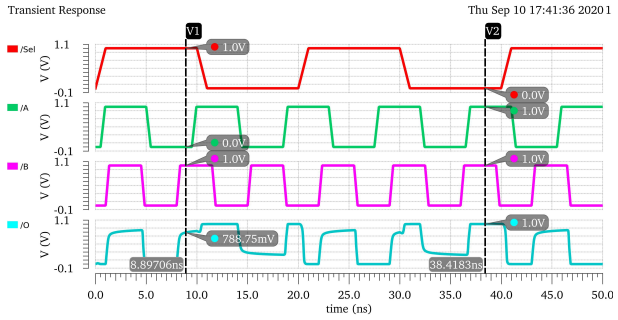
The structure of TG, MSL, Static CMOS, CPL, and CVSL is such that they can transfer perfect 0 V or 1 V to the output whenever the select lines permit. Therefore, their output waveforms obtained are ideal. The ideal output waveform is given in Fig. 3(a). The ideal output situation is not attained for GDI based multiplexer, as showcased in Fig. 3(b). The GDI based multiplexer is designed using a pair of NMOS and PMOS. When the input at PMOS is 0, the output is not a perfect 0, as PMOS delivers a weak 0. Similarly, when input is 1 at NMOS, the output obtained is not equivalent to 1 as NMOS provides weak 1 at the output. The other multiplexer structure unable to produce ideal output is PT based multiplexer. This is the case as the schematic for PT based multiplexer is purely dependent on NMOS for the generation of output. As a result, the structure can never pass a perfect 1 due to NMOS being a weak 1. This technique produces a perfect 0 V level but the 1 V output level always falls short of its perfect value, as can be observed in Fig. 3(c).

Lastly, the output obtained for MTCMOS CVLS is different in comparison to all other multiplexer structures, as depicted in Fig. 3(d). This technique is dependent on an additional pair of PMOS-NMOS, of which the PMOS transistor is used to isolate the V_{DC} from the circuit and the NMOS transistor is used to isolate the ground. This is done to reduce the power dissipation of the circuit. But this has its implications on the output waveforms. When sleep = 0, the circuit works as expected of a multiplexer circuitry, but when sleep = 1, the multiplexer circuit gets isolated from supply voltage and ground. The output is put in high-impedance state, losing the driving capabilities. This occurs as the entire circuit is disconnected from the supply voltage and ground. On the other side,

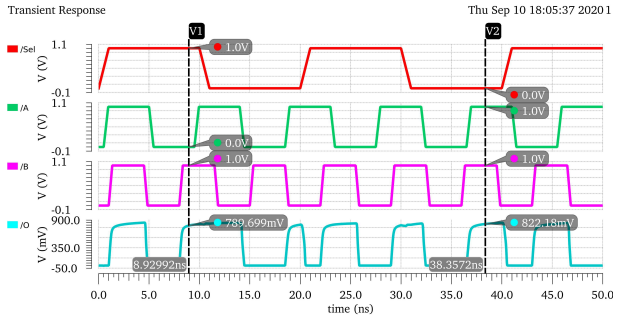
when the sleep signal is low, the connections to the supply voltage and ground are re-established for the multiplexer core. Thus, the circuit produces output in keeping with the functioning of a multiplexer circuit.



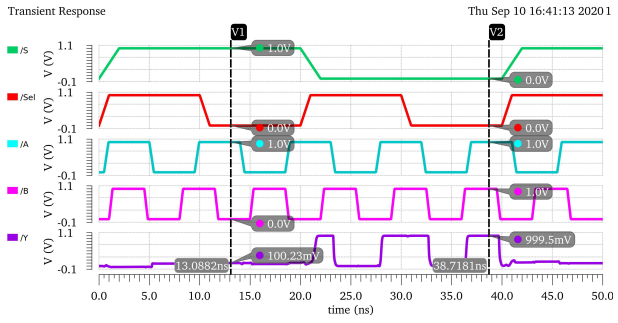
(a) Ideal scenario.



(b) GDI multiplexer.



(c) PT multiplexer.



(d) MTCMOS CVSL multiplexer.

Fig. 3: The output response for ideal scenario, GDI multiplexer, PT multiplexer and MTCMOS CVSL multiplexer.

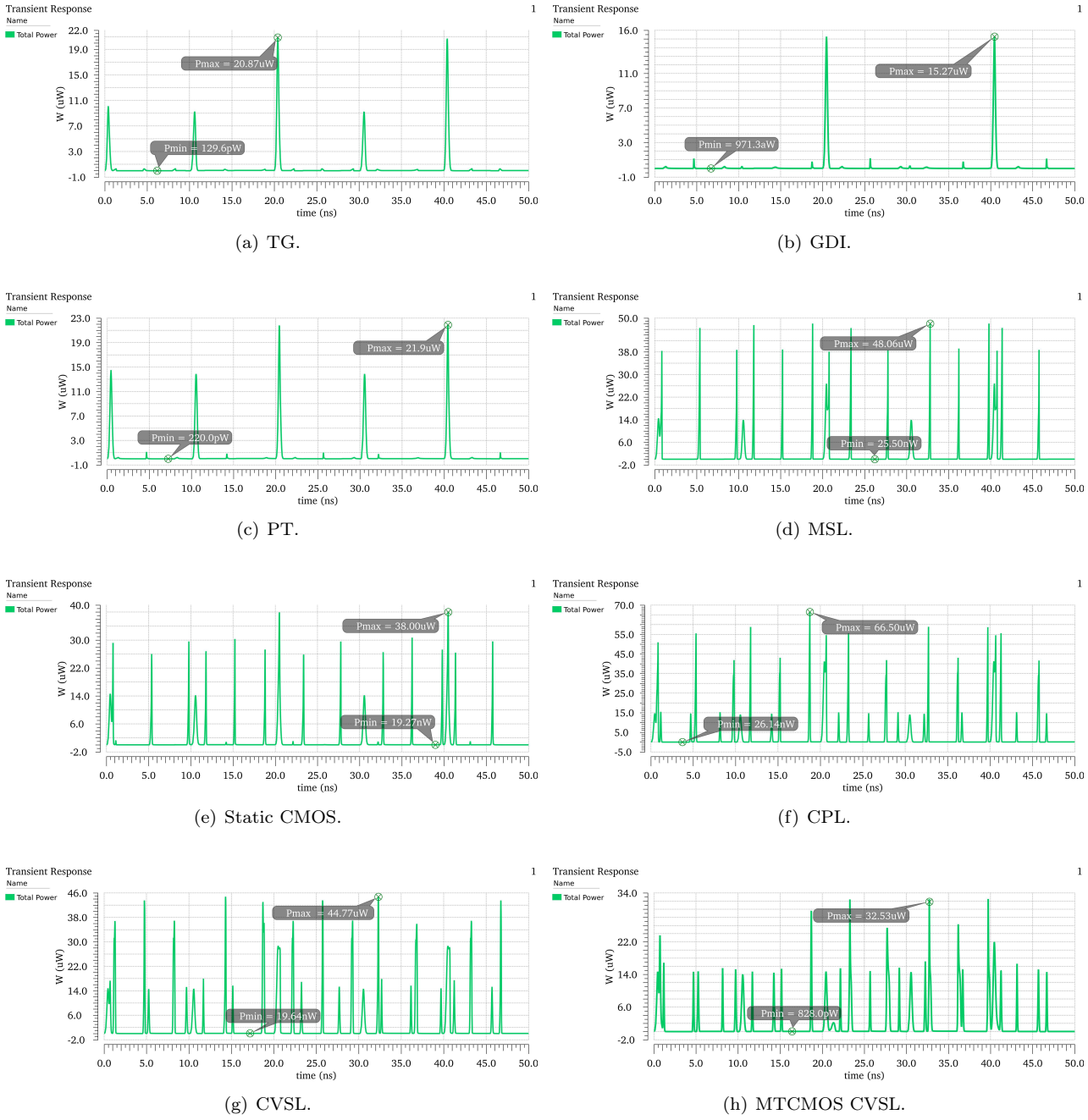
4. Dynamic Power Dissipation Analysis

Power dissipation is a key characteristic of all considered structures. With the increasing popularity of low-power devices, it has become imperative to study the power dissipation of all multiplexer techniques as well. In Fig. 4, the dynamic power dissipation pulses corresponding to the output wave pulse are presented for different multiplexer techniques. Dynamic power consumption is caused by current flow in circuit, when the transistors of the devices are switching from one logic state to another. The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the number of internal nodes on the critical path for the device, have a direct effect on the duration of the current spike [27].

To measure the power dissipation for the multiplexers, a test wave was applied to all and the power dissipation was measured from the output waveform generated at the output node. The maximum and minimum power dissipation of TG, GDI, PT, MSL, Static CMOS, CPL, CVSL and MTCMOS CVSL based multiplexer are depicted in Tab. 1. The maximum power dissipation of MSL based multiplexer is obtained as 463.59 µW, which is observed least amongst all other multiplexers, as demonstrated in Tab. 1. On the other hand, the obtained power dissipation is minimum for GDI based multiplexer with a magnitude of 9.7 fW, which is reduced by order of 5 as compared to TG, PT and MTCMOS CVSL based multiplexer and decreased by order of 7 than that of MSL, Static CMOS, CPL and CVSL based multiplexers. The average power dissipation of PT based multiplexer is achieved as 537.1 nW, which is the lowest amongst all other multiplexers, as shown in Tab. 1.

Having explained the maximum, minimum and average power consumption for different configurations for the ease of inter-technique comparison, the values are tabulated in Tab. 1 and Tab. 2. As can be noticed from Tab. 1, the maximum power consumption is least for the MSL technique at 463.59 µW. However, the minimum power consumption for this technique is significantly high. The least minimum power consumption is observed for GDI based technique at 9.71 fW, but its maximum power consumption is the highest of all.

Another parameter, average power dissipation, is used to characterize the multiplexer structures. All the inputs are switching at different time instance, so the current will also be different at each time, which leads to different power dissipation value [28]. The average power is proportional to the energy required to charge and discharge the circuit capacitance. This power dissipation parameter is dependent on



(a) TG. (b) GDI.

(c) PT. (d) MSL.

(e) Static CMOS. (f) CPL.

(g) CVSL. (h) MTCMOS CVSL.

Fig. 4: Dynamic power dissipation for TG, GDI, PT, MSL, Static CMOS, CPL, CVSL and MTCMOS CVSL.

Tab. 1: Total and average power dissipation.

Multiplexer configuration	Maximum power dissipation (μW)	Minimum power dissipation (nW)	Average power dissipation (μW)
TG	523.36	0.1296	0.642
GDI	587.34	0.00000971	2.065
PT	493.74	0.22	0.5371
MSL	463.59	25.50	1.73
Static CMOS	478.63	19.27	1.305
CPL	579.63	26.14	3.01
CVSL	556.32	19.64	2.88
MTCMOS CVSL	527.8	0.828	1.93

Tab. 2: Percentage analysis.

Multiplexer configuration	Percentage reduction in maximum power dissipation (μW) of MSL based multiplexer as compared to other multiplexer	Percentage reduction in average power dissipation (μW) of PT based multiplexer as compared to other multiplexer
TG	11.42 %	16.33 %
GDI	21.06 %	73.99 %
PT	6.106 %	—
MSL	—	68.95 %
Static CMOS	3.14 %	58.54 %
CPL	20.01 %	82.15 %
CVSL	16.66 %	81.35 %
MTCMOS CVSL	12.13 %	72.17 %

Tab. 3: Percentage analysis.

Multiplexer configuration	Delay (ps)	Average power (μW)	PDP (aJ)	Static power dissipation (nW)
Conventional TG	14.34 (A to O) 15.3 (B to O)	0.642	0.00981	98.63
GDI	18.49 (A to O) 15.38 (B to O)	2.065	0.0794	0.689
PT	14.83 (A to O) 14.79 (B to O)	0.5371	0.00796	102.86
MSL	55.12 (A to O) 56.64 (B to O)	1.73	0.0962	104.22
Static CMOS	51.24 (A to O) 54.68 (B to O)	1.305	0.0713	105.98
CPL	103.0 (A to O) 95.66 (B to O)	3.01	0.31	210.75
CVSL	166.3 (A to O) 151.8 (B to O)	2.88	0.478	162.62
MTCMOS CVSL	303.9 (A to O) 295.7 (B to O)	1.93	0.586	167.68 (S = 0) 78.95 (S = 1)

the switching frequency but is independent of the device parameters.

The average power dissipation is found least for PT based structure at 537.1 nW. The interesting thing to observe about the PT structure is its moderate maximum and minimum power. They are neither too high nor too low, making it the ideal technique in terms of power dissipation performance.

5. Delay and Power Analysis

The necessities of multiplexer for better performance include short propagation time and total power consumption, while static power dissipation ought to be minimum. The selection of multiplexer depends on the requirement of either propagation delay or power consumption. Table 3 explains the analysis of Delay, Average Power, PDP and Static Power Dissipation. By analysing the delay and power of different multiplexers, it is evident that the performance of each multiplexer is different, moreover, two of them presenting better performance compared to others in terms of propagation time, power consumption and leakage current.

Table 3 reveals that the propagation delay of TG based multiplexer is the shortest. For static condition, GDI based multiplexer outperforms with less amount of minimum power dissipation. Additionally, it dissipates minimum static power of 689 pW. On the other side, PT based multiplexer is slower by the value of 0.49 ps than TG multiplexer but it shows the lowest average power dissipation of 537.1 nW. In some condition, PDP of the circuit is considered as an important characteristic which ought to be minimum. Subsequently, the PDP of PT based multiplexer is minimum with a magnitude of 0.00796 aJ, thereby PT based multiplexer shows the optimum performance.

6. Conclusion

Eight structures of multiplexer implementation have been analysed for dynamic power consumption, delay, static power and power delay product. The maximum and minimum power dissipation are illustrated in Tab. 1. If average power dissipation is considered, then PT based multiplexer has achieved the best performance at 537.1 nW. The delay analysis recommends TG based multiplexer as the fastest multiplexer as it has the least delay recorded at 14.34 ps. Additionally, GDI based multiplexer registers the minimum static power dissipation of 689 pW. While in terms of average power dissipation, PT based multiplexer outperforms

TG based multiplexer but it is slower by the value of 0.49 ps than the TG multiplexer. The results obtained above strongly suggest that each multiplexer technique has its own merits. Some techniques demonstrate excellent power performance, while the other have faster operations, or are better at static performance. We believe that this comparison will be helpful for right choice of multiplexers in the design structure according to switching requirements, power consumption and occupied area.

Author Contributions

N.K. and P.M. conceived the idea and planned the complete work. N.K. has carried out all the simulations and plotted/analyzed all the results. M.M. and P.M. performed the calculations and analysed the data. B.R. and M.M. contributed to the interpretation of the results and modified the graphs. M.M. and B.R. designed the model and the computational framework. M.M. and N.K. drafted first write-up of the manuscript. P.M. and B.R. prepared the first revised manuscripts. B.R. and P.M. prepared the detailed Response to the Reviewer comments. M.M. and N.K. carried out the implementation and amended the modifications in the manuscript. M.M., N.K., B.R. and P.M. prepared second, third and fourth revised manuscripts. All authors provided critical feedback and helped shape the research, analysis and manuscript.

References

[1] SINGH, U., L. LI and M. M. GREEN. A 34 Gb/s Distributed 2:1 MUX and CMU using 0.18 µm CMOS. *IEEE Journal of Solid State Circuits*. 2006, vol. 41, iss. 9, pp. 2067–2076. ISSN 1558-173X. DOI: 10.1109/JSSC.2006.880630.

[2] CHEN, F.-T., J.-M. WU and M.-C. FRANK CHANG. 40-Gb/s 0.7-V 2:1 MUX and 1:2 DEMUX with Transformer-Coupled Technique for SerDes Interface. *IEEE Transactions on Circuits and Systems I: Regular Papers*. 2015, vol. 62, iss. 4, pp. 1042–1051. ISSN 1558-0806. DOI: 10.1109/TCSI.2015.2395634.

[3] MITTAL, P., Y. S. NEGI and R. K. SINGH. Impact of source and drain contact thickness on the performance of organic thin film transistors. *Journal of Semiconductors*. 2014, vol. 35, iss. 12, pp. 1–7. ISSN 1674-4926. DOI: 10.1088/1674-4926/35/12/124002.

[4] HAFIZ, M. A. A., L. KOSURU, M. I. YOUNIS and H. FARIBORZI. A 2:1 MUX Based on Multiple MEMS Resonators. *Procedia Engineering*. 2016, vol. 168, iss. 1, pp. 1642–1645. ISSN 1877-7058. DOI: 10.1016/j.proeng.2016.11.480.

[5] ETEZADI, S. and S. A. HOSSEINI. Novel Ternary Logic Gates Design in Nanoelectronics. *Advances in Electrical and Electronic Engineering*. 2019, vol. 17, iss. 3, pp. 294–305. ISSN 1804-3119. DOI: 10.15598/aeee.v17i3.3156.

[6] YAN, Z., W. ZHIGONG and L. WEI. 80 Gb/s 2:1 Multiplexer in 0.13-µm SiGe BiCMOS Technology. *Journal of Semiconductors*. 2009, vol. 30, iss. 2, pp. 1–4. ISSN 1674-4926. DOI: 10.1088/1674-4926/30/2/025008.

[7] CHANGCHUN, Z., W. ZHIGONG, S. SI, M. PENG and T. LING. 5-Gb/s 0.18-µm CMOS 2:1 multiplexer with integrated clock extraction. *Journal of Semiconductors*. 2009, vol. 30, iss. 9, pp. 1–6. ISSN 1674-4926. DOI: 10.1088/1674-4926/30/9/095009.

[8] MAJUMDER, A., M. DAS, S. K. SAW and B. K. BHATTACHARYYA. An energy efficient PVT aware novel CML-TG based mux-latch circuit serializes high rate data. *Microsystem Technologies*. 2021, vol. 27, iss. 2, pp. 555–568. ISSN 1432-1858. DOI: 10.1007/s00542-018-4093-x.

[9] JAIN, P. and S. AKASHE. Power delay optimization of nanoscale 4x1 multiplexer using CMOS based voltage doubler circuit. *Radioelectronics and Communications Systems*. 2016, vol. 59, iss. 11, pp. 477–488. ISSN 1934-8061. DOI: 10.3103/S0735272716110017.

[10] DIXIT, A., S. KHANDELWAL and S. AKASHE. Power Optimization of 8:1 MUX using Transmission Gate Logic (TGL) with Power Gating Technique. *International Journal of Computer Applications*. 2014, vol. 99, iss. 5, pp. 37–42. ISSN 2250-1797. DOI: 10.5120/17373-7911.

[11] MISHRA, M. and S. AKASHE. High performance, low power 200 Gb/s 4:1 MUX with TGL in 45 nm technology. *Applied Nanoscience*. 2014, vol. 4, iss. 3, pp. 271–277. ISSN 2190-5517. DOI: 10.1007/s13204-013-0206-0.

[12] PONNIAN, J., S. PARI, U. RAMADASS and O. C. PUN. A New Systematic GDI Circuit Synthesis Using MUX Based Decomposition Algorithm and Binary Decision Diagram for Low Power ASIC Circuit Design. *Microelectronics Journal*. 2021, vol. 108, iss. 1, pp. 1–23. ISSN 0026-2692. DOI: 10.1016/j.mejo.2020.104963.

[13] MORGENSHTEIN, A., V. YUZHANINOV, A. KOVSHILOVSKY and A. FISH. Full-Swing Gate Diffusion Input logic—Case-study of low-power CLA adder design. *Integration*. 2014, vol. 47, iss. 1, pp. 62–70. ISSN 0167-9260. DOI: 10.1016/j.vlsi.2013.04.002.

[14] MORGENSHTEIN, A., A. FISH and I. A. WAGNER. Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits. *IEEE Transactions On Very Large Scale Integration (VLSI) Systems*. 2002, vol. 10, iss. 5, pp. 566–581. ISSN 1557-9999. DOI: 10.1109/TVLSI.2002.801578.

[15] YANO, K., T. YAMANAKA, T. YISHIDA, M. SAITO, K. SHIMOHIGASHI and A. SHIMIZU. A 3.8-ns CMOS 16*16-b multiplier using complementary pass-transistor logic. *IEEE Journal of Solid State Circuits*. 1990, vol. 25, iss. 2, pp. 388–395. ISSN 1558-173X. DOI: 10.1109/4.52161.

[16] PASTERNAK, J. H., A. S. SHUBAT and C. A. T. SALAMA. CMOS differential pass-transistor logic design. *IEEE Journal of Solid State Circuits*. 1987, vol. 22, iss. 2, pp. 216–222. ISSN 1558-173X. DOI: 10.1109/JSSC.1987.1052705.

[17] SUZUKI, M., N. OHKUBO, T. SHINBO, T. YAMANAKA, A. SHIMIZU, K. SASAKI and Y. NAKAGOME. A 1.5-ns 32-b CMOS ALU in double pass-transistor logic. *IEEE Journal of Solid State Circuits*. 1993, vol. 28, iss. 11, pp. 1145–1151. ISSN 1558-173X. DOI: 10.1109/4.245595.

[18] YANO, K., Y. SASAKI, K. RIKINO and K. SEKI. Top-down pass-transistor logic design. *IEEE Journal of Solid-State Circuits*. 1996, vol. 31, iss. 6, pp. 792–803. ISSN 1558-173X. DOI: 10.1109/4.509865.

[19] HU, X., A. S. ABRAHANM, J. A. C. INCORVIA and J. S. FRIEDMAN. Hybrid Pass Transistor Logic with Ambipolar Transistor. *IEEE Transactions on Circuits and Systems I: Regular Papers*. 2021, vol. 68, iss. 1, pp. 301–310. ISSN 1558-0806. DOI: 10.1109/TCSI.2020.3034042.

[20] GUPTA, I., N. ARORA and B. P. SINGH. Simulation and analysis of 2:1 multiplexer circuits at 90nm technology. *International Journal of Modern Engineering Research*. 2011, vol. 1, iss. 2, pp. 642–647. ISSN 2249-6645.

[21] YANG, C. and M. CIESIELSKI. Synthesis for mixed CMOS/PTL logic. In: *Proceedings Design, Automation and Test in Europe Conference and Exhibition*. France: IEEE, 2000, pp. 750. ISBN 0-7695-0537-6. DOI: 10.1109/date.2000.840883.

[22] PATEL, S. K., B. GARG and S. K. RAI. A power and area mux efficient approximate carry skip adder for rror resilient application. *Turkish Journal of Electrical Engineering & Computer Sciences*. 2019, vol. 528, iss. 1, pp. 443–457. ISSN 0167-9260. DOI: 10.3906/elk-1907-72.

[23] PAL, P. K. and R. K. NAGARIA. A Low-Power Low-Supply MOS-Only Subthreshold Voltage Reference for Wide Temperature Range. *Advances in Electrical and Electronic Engineering*. 2019, vol. 17, iss. 2, pp. 167–178. ISSN 1804-3119. DOI: 10.15598/aeee.v17i2.3197.

[24] HATANO, H. Single Event Effects on Static and Clocked Cascade Voltage Switch Logic (CVSL) Circuits. *IEEE Transactions on Nuclear Science*. 2009, vol. 56, iss. 4, pp. 1987–1991. ISSN 1558-1578. DOI: 10.1109/TNS.2009.2015663.

[25] JIAO, H. and V. KURSUN. Mode transition timing and energy overhead analysis in noise-aware MTCMOS circuits. *Microelectronics Journal*. 2014, vol. 45, iss. 8, pp. 1125–1131. ISSN 0026-2692. DOI: 10.1016/j.mejo.2014.05.006.

[26] DAS, M., A. MAJUMDER, A. J. MONDAL and B. K. BHATTACHARYYA. A 90nm Novel MUX-Dual Latch Design Approach for Gigascale Serializer Application. In: *2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*. Bhopal: IEEE, 2017, pp. 210–214. ISBN 978-1-5386-1356-6. DOI: 10.1109/iNIS.2017.46.

[27] MISHRA, N., P. MITTAL and B. KUMAR. Analytical modeling for static and dynamic response of organic pseudo all-p inverter circuits. *Journal of Computational Electronics*. 2019, vol. 18, iss. 4, pp. 1490–1500. ISSN 1572-8137. DOI: 10.1007/s10825-019-01400-9.

[28] NADOOSHAN, R. S. and M. KIANPOUR. A novel QCA implementation of MUX-based universal shift register. *Journal of Computational Electronics*. 2014, vol. 13, iss. 1, pp. 198–210. ISSN 1572-8137. DOI: 10.1007/s10825-013-0500-9.

About Authors

Nishant KUMAR was born in Firozabad, India in 1993. He received his B.Tech. Degree in Electronics and Communication Engineering with 67.04 %

from Ajay Kumar Garg Engineering College, Ghaziabad, India in 2015. He has received his M.Tech. degree with CGPA of 8.46 from Delhi Technological University, New Delhi, India. His research interests include low power circuit design, memory circuits in emerging technologies.

Poornima MITTAL (Ph.D., M.Tech., B.Tech.), Member IEEE has published 110+ research papers in international journals and conferences of repute. Her research interest includes design/modeling of flexible electronic devices, thin film fabrication, memory and low power very large scale integration circuits. She has published one patent and a Text Book titled "Organic Thin-Film-Transistor Applications: Materials to Circuits" by CRC Press, Taylor & Francis in 2016. She is the reviewer of Institute of Electrical and Electronics Engineers (IEEE) transactions and other reputed international journals of IEEE, Institution of Engineering and Technology (IET), Elsevier, Institute of Physics Publishing (IOP), Wiley and Taylor & Francis. She has received the research awards in 2012, 2015, 2019, 2020 and 2021. She has delivered many expert talks and chaired sessions in the reputed international conferences. She is the life member of many professional societies. She has more than 15 years of academic and research experience. Presently, she is working as Professor in the Department of Electronics and Communication Engineering at Delhi Technological University, Delhi, India.

Bhawna RAWAT (M.Tech., B.Tech.) was born in Delhi, India in 1993. She received her B.Sc. Degree in Electronics and Communication Engineering from Shiv Nadar University, Greater Noida, India in 2015. She received M.Sc. degree in VLSI Design from Indira Gandhi Delhi Technical University for Women, Delhi, India. She is presently pursuing Ph.D. at Delhi Technical University, New Delhi, India. Her research interests include low power circuit design, memory circuits in emerging technologies.

Mudit MITTAL (M.Tech., MCA) is presently working as the Head of CS/IT Department, Institute of Technology and Management, Dehradun (Uttarakhand). He has 12 years rich experience of academics. His area of interest includes Digital Electronics, Automata Technology, Programming, Algorithm Analysis, Graph Theory and Data Structures. He has many international and national research publications.