# The Influence of Repetitive UIS on Electrical Properties of Advanced Automotive Power Transistors

*Juraj MAREK* [1], *Jozef KOZARIK* [1,2], *Michal MINARIK* [1], *Ales CHVALA* [1], *Lubica STUCHLIKOVA* [1]

[1]Institute of Electronics and Photonics, Slovak University of Technology in Bratislava, Ilkovicova 3, 812 19 Bratislava, Slovak Republic
[2]NanoDesign, s.r.o, Drotarska 19a, 811 04 Bratislava, Slovak Republic

juraj.marek@stuba.sk, jozef.kozarik@stuba.sk, michal_minarik@stuba.sk, ales.chvala@stuba.sk, lubica.stuchlikova@stuba.sk

DOI: 10.15598/aeee.v20i1.4120

Article history: Received Feb 22, 2021; Revised Nov 08, 2021; Accepted Nov 23, 2021; Published Mar 31, 2022.


***Abstract.*** *This paper investigates a degradation of three types of automotive power MOSFETs through repetitive Unclamped Inductive Switching (UIS) test typically used to evaluate the avalanche robustness of power devices. It is not uncommon in switching applications that greater than the planned voltage for voltage spikes can occur, so even the best electronic designs may encounter frequent avalanche events. Hence, there is a need to analyse the impact of repetitive avalanching on the electrical performance of power transistors. This article focused on the shift of main electrical parameters: on-resistance $R_{ON}$, breakdown voltage $V_{BR}$, threshold voltage $V_{TH}$, and corresponding characteristics, as well as capacitances. Analysis proved that DMOS transistors are less vulnerable to repetitive avalanching. The most impacted parameter was on-resistance $R_{DSon}$, where a 14 % increase was observed after $6 \cdot 10^7$ stress pulses. The parameters shift is attributed to hot carrier injection in the space charge region of blocking PN junction and involves mainly defects generation/activation in the drain side region of the gate oxide. For the TrenchMOS transistor, a significant shift of $I-V$ curves was observed with considerable impact on the $R_{ON}$ where an increase of 22 % was observed. The trench corner is verified to be the mainly degraded region by Synopsys Technology Computer Aided Design (TCAD) simulations. Degradation of drain-gate capacitance $C_{DG}$ and input capacitance $C_{in}$ was observed in all three types of analysed structures. DLTS was used to verify the generation/activation of defects invoked by stress. An increase of DLTS signal corresponding to energy levels of oxygen vacancies and impurities in $SiO_2$ and on interfaces were detected on stressed samples.*

## Keywords

***Degradation, DLTS, repetitive avalanching, repetitive Unclamped Inductive Switching (UIS), TCAD.***

## 1. Introduction

Silicon power MOSFETs have still a dominant role in automotive and industrial electronics where the power devices drive relatively high inductive loads [1], [2], and [3]. Therefore, high voltage and high current operations are common requirements for semiconductor devices in power applications [4], [5], and [6]. When a power MOSFET is used in circuit application, an unclamped inductive load presents extremely stressful switching condition. During the switching all of the energy stored in the inductor during on state is dumped directly into the device during its turn off typically by driving it into avalanche mode conduction [4], [7], [8], and [9]. As a consequence, the ability of the MOSFET to withstand instances of Unclamped Inductive Switching (UIS) is an important performance metric.

Thus, a UIS test condition represents the circuit switching operation for evaluating the avalanche ruggedness of the device [10], [11], and [12]. Typically, a standard UIS test described by JEDEC standards is a single pulse test, but power MOSFETS in real automotive systems can be subjected to events of UIS over the lifetime of their application. Therefore, standard UIS tests cannot fully reveal possible risks arising from repetitive avalanche operations [13] and [14].

An excellent example of an application where repetitive avalanching occurs is the antilock braking system. The system is typically composed of a low-side power MOSFET switch that connects the brake pump to the battery and is switched by a pressure control system connected to the gate [15]. Every time the MOSFET is switched on, the brake pump is connected to the battery and energy is stored in the inductors of the brake pump. When the MOSFET is switched off, the energy in the brake pump is dissipated through the MOSFET by driving it into the avalanche and this event can occur over 500 million times in the operating life of the vehicle's automotive system [15].

During avalanching, High Concentrations of hot electron-hole pairs (HC) are generated in close proximity of blocking PN junction and gate interfaces [16]. Due to high kinetic energy, hot carriers can be injected and get trapped in insulating layers and interfaces. They are able to break atomic bonds thereby creating interface states or electrically activating defects. This may lead to the change of threshold voltage $V_{TH}$, breakdown voltage $V_{BR}$, and on-resistance $R_{ON}$ [14]. These changes during the lifetime operation of the device pose considerable risks against the requirement of long-term reliability of automotive power MOSFETs.

## 2. UIS Test

A custom-built avalanche test equipment (Fig. 1(a)) was used for repetitive ruggedness testing to perform more than $10^8$ stress pulses. A commercial UIS tester ITC55100 was used for reference measurements and calibration. Commercial tester is not suitable for long-term measurements because each set of 100 pulses is followed by the time period needed for communication. This represents a considerable delay for a larger number of pulses.

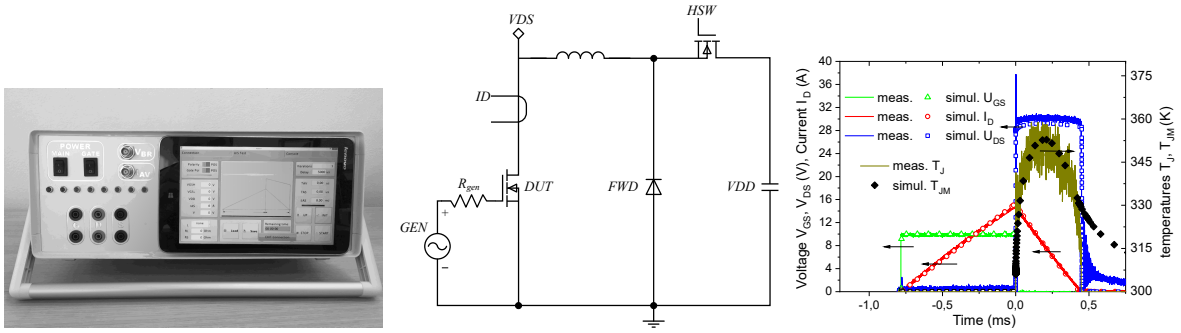
In Fig. 1(b) the circuit diagram and typical voltage and current waveforms during the test are shown. The test circuit conditions (Fig. 1(b)) were defined by following parameters: supply voltage $V_{DD} = 20$ V, peak inductance current $I_{AS} = 5$ A, inductive load $L = 1$ mH, max gate voltage $V_G = 10$ V, and gate resistance $R_{Gen} = 25\ \Omega$. The duty cycle was set to 10 % to maintain temperature of tested device under 130 °C controlled by an IR camera. The Device Under Test (DUT) is connected to the power supply through the inductor and high side switch HSW. When both DUT and HSW are turned ON, current, limited by the inductor, starts to rise linearly. When the current through inductance reaches the preset value $I_{AS}$, DUT and HSW are turned off by the control unit, and the $V_{DD}$ source is disconnected from the test circuit, therefore active part of the test circuit now consists only of the DUT, charged inductive load $L$, and FWD diode.

As DUT is turning off, the current through the transistor channel is decreasing until the channel is completely closed. However, the current through inductance cannot change instantaneously. Therefore, the magnetic field of charged inductor induces a counter Electromagnetic Force (EMF) against this change to keep current flowing through inductor. EMF induces high potential across the inductor and DUT which drives DUT to the electric breakdown [8]. Current from the inductor now flows through DUT as an avalanche current, and the current loop is closed by the FWD diode. If no protective circuits are added in parallel to the switch, all build-in energy of the inductor is dissipated directly into the device [12].

Different types of automotive-grade MOSFETS were used for investigations: vertical DMOS rated to 24 V and two Trench MOS transistors rated to 30 V and 90 V. To analyze parameter degradation, $I-V$ and $C-V$ measurements were performed first on virgin samples, and then after each set of stress pulses. To support the analysis of parameter shift due to HCI, TCAD simulations and modeling were performed. Deep Level Transient Spectroscopy (DLTS) measurements were accomplished to analyze parameters and the possible origin of generated/activated electrically active defects.

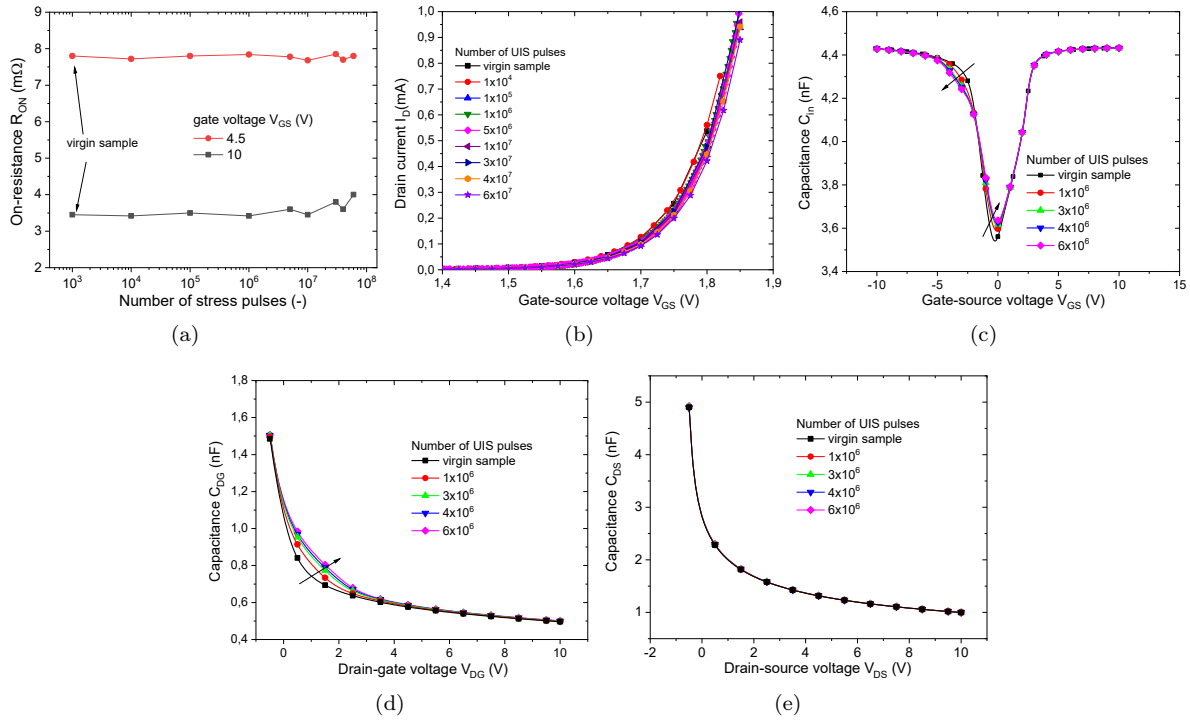
## 3. Results and Discussion

First, DMOS transistors were subjected to repetitive UIS stress for up to $6 \cdot 10^7$ of stress pulses. Measured on-resistance $R_{ON}$, transfer and $C-V$ characteristics are shown in Fig. 2. The impact of stress on $I-V$ characteristics was very low and non-uniform. Increase by 14 % of on- resistance was observed after $6 \cdot 10^7$ of stress pulses. We assume that the increase of on-resistance can be more attributed to the material degradation (degradation of the top side metallization due to the cyclic thermal stress) than to the degradation of channel $Si/SiO_2$ interface caused by HCI [13], [14] and [15].




(a) (b) (c)

**Fig. 1:** (a) Custom-built repetitive avalanche test equipment. (b) Basic UIS test circuit and (c) typical waveforms of current, voltage and junction temperature of the DUT under UIS test conditions.

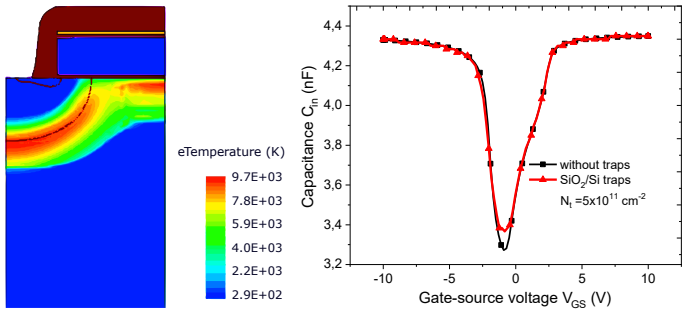



(a) (b) (c) (d) (e)

**Fig. 2:** DMOS transistor - impact of repetitive UIS stress on shift of electrical parameters and characteristics: (a) on on-resistance $R_{ON}$, (b) transfer characteristics, (c) input capacitance $C_{in}$, (d) drain to gate capacitance $C_{DG}$ and (e) drain to source capacitance $C_{DS}$.

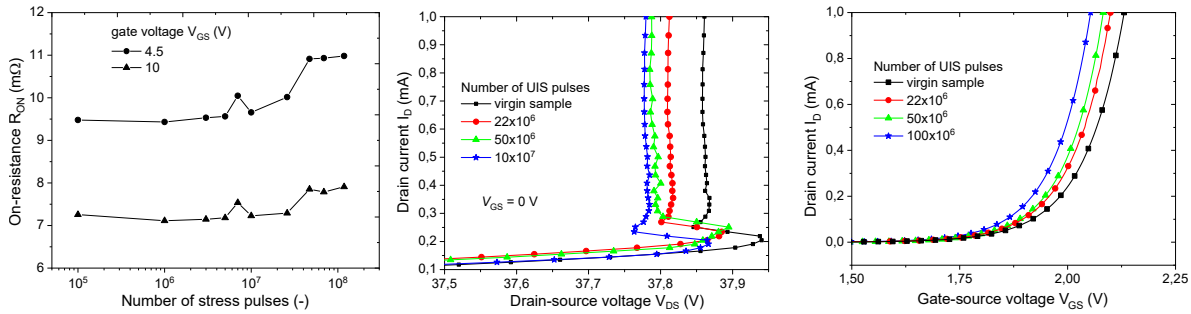
It is a well-known fact that long-term thermal cycling leads to degradation of top metalization. Degradation of power metal leads to increased serial resistance of transistor but has minimal effect on $C-V$ characteristics. Our assumptions are also confirmed by the fact that only a small change in the threshold voltage was observed. From $C-V$ measurements (Fig. 2(c), Fig. 2(d) and Fig. 2(e)), it is clear that the most considerable impact of applied stress was observed for capacitances $C_{IN}$ and $C_{GD}$ whilst shift of drain to source capacitance $C_{DS}$ was negligible. Change of capacitances $C_{IN}$ and $C_{GD}$ was saturated after $6 \cdot 10^6$ of stress pulses, and no further change was observed. This is in good correlation with results observed in published works [16], [17], [18], and [19].

To explain the shift of gate to drain capacitance, TCAD simulations in Synopsys TCAD were performed to visualize the location and distribution of hot electrons in the device's volume at the beginning of the discharging period when the highest voltage and current are present on the device (Fig. 3(a)). For this reason, hydrodynamic simulations were performed using the University of Bologna (UniBo) model for avalanche generation. Models of structures (for DMOS as well as TrenchMOS) were generated from simulation




(a) (b)

**Fig. 3:** (a) Distribution of hot electrons in the volume of DMOS transistor during the avalanching period of UIS test. (b) Simulated CV curves with defined traps on $SiO_2/Si$ interface on the drain side of the gate electrode.




(a) (b) (c)

**Fig. 4:** TrenchMOSFET - Impact of repetitive UIS stress on shift electrical parameters and characteristics: (a) on on-resistance RON, (b) breakdown and (c) transfer characteristics.

of technological processes provided by samples manufacturer. This also ensured a good match of simulated and real characteristics.

Most of the generated hot carriers at the bottom of the P-well are sufficiently far from the transistor channel; therefore, their influence on threshold voltage and on-resistance is limited. Only a small amount of HC is close to the gate dielectric. Injection of HC to the gate dielectric in this part of the structure is therefore responsible for the change of $C_{IN}$ and $C_{GD}$ capacitances. This was verified by TCAD simulation with added traps (fixed charge $N_t = 5 \cdot 10^{11}$ cm$^{-2}$) to the $SiO_2/Si$ interface in the exposed part of the structure (Fig. 3(b)).

Furthermore, 30 V Trench MOSFETs were subjected to repetitive UIS test. In this case shift of transfer and breakdown characteristics were observed (Fig. 4) as well as a small increase of on-resistance. Performed TCAD simulations indicate that the drain side of the gate dielectric and channel area is more exposed to hot electrons generated during the avalanching period of the test (Fig. 5). Therefore, the shift of the characteristics and parameters is more significant than in the case of DMOS transistors. The fact that different increase of on-resistance was observed for different gate potentials indicates HCI origin of on-resistance degradation. We think that, in our case, metal degradation invoked by thermomechanical stress during temperature excursions from avalanche pulses was negligible [20], [21], [22], and [23]. Degradation of source metal would cause the increase of metal serial resistance independent from gate voltage. To simulate the impact of trapped/injected charge in the $SiO_2/Si$ interface, simulations with defined positive fix charge were performed. Fix charge was defined only on the small part of the $SiO_2/Si$ interface (critical area) where high concentrations of hot holes are present during the avalanching period. The results are shown in Fig. 5(b).

Last analyzed devices were 90 V rated TrenchMOS transistors; the results are shown in Fig. 6. Whilst in the case of the 30 V devices, only a small impact of repetitive UIS on the $V_{BR}$ was observed, in the case of 90 V rated devices, impact on the $V_{BR}$ voltage dominates for the first million pulses and then it saturates on the value $V_{BR} = 98$ V (Fig. 6(b)). The impact of repetitive avalanching on the on-resistance $R_{ON}$ and transfer characteristic was initially minimal, but for the higher number of stress pulses it becomes more significant (Fig. 6(a) and Fig. 6(c)). To ensure high breakdown voltage and low on-resistance, more deep trenches with superjunction technology are

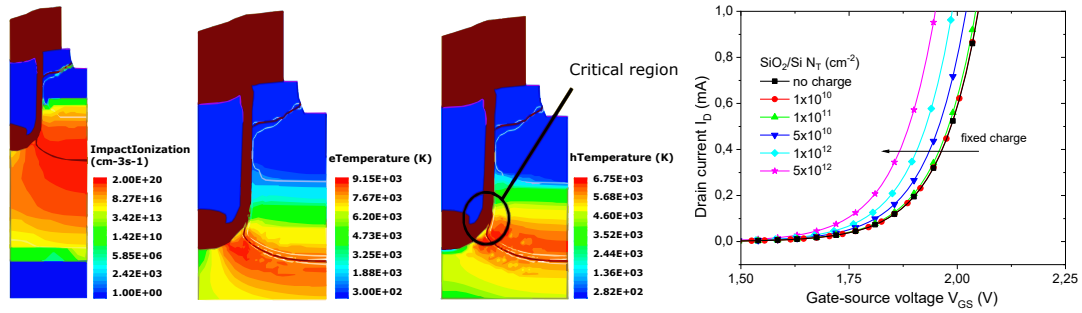



**Fig. 5:** (a) Distribution of impact ionization, hot electrons and holes during the avalanching period in TrenchMOS. (b) Simulated impact of interface charge on transfer characteristics.

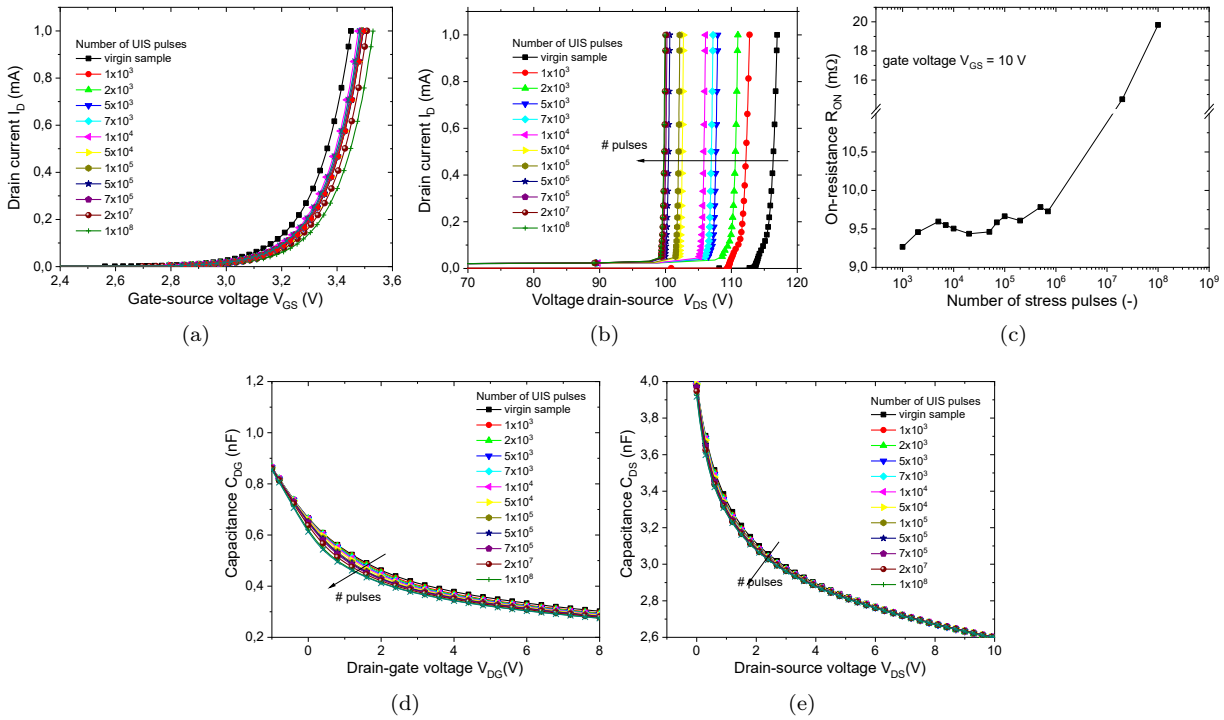


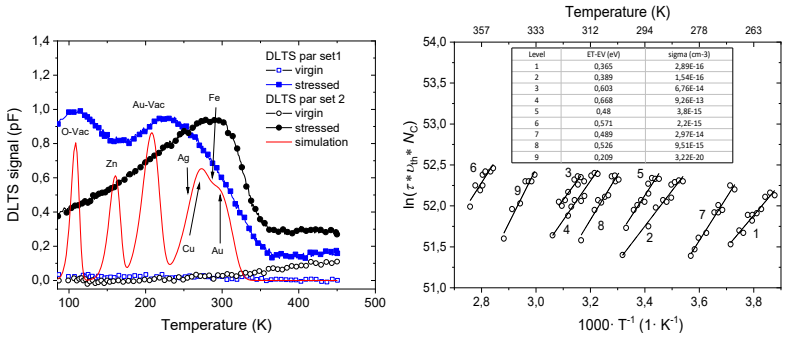

**Fig. 6:** Repetitive UIS invoked shift of electrical parameters and characteristics of 90V rated Trench MOSFET: (a) breakdown voltage, (b) transfer characteristic, (c) on resistance, (d) drain-gate capacitance and (e) drain-source capacitance.

used in high and middle voltage range Trench MOSFET technology [8]. Breakdown typically occurs at the same depth as the bottom of the trench. Therefore, channel area and the gate oxide dielectric are only affected by a small amount of generated hot carriers. Therefore, higher number of stress pulses is needed to invoke change of the transfer characteristic or on-resistance. On the other hand, the value of the breakdown voltage in super junction structures strongly depends on the additional charge that may disrupt the charge balance and therefore decrease the value of breakdown voltage.

To analyze the generated/activated traps, DLTS study was performed using DLTFS system Bio-Rad DL 8000. Measurements were performed on 30 V Trench-MOS transistors using $C_{GD}$ capacitance and different sets of parameters. Measured spectra confirm the large number of defects generated or activated on the drain side of the gate oxide due to hot carrier injection. Observed DLTS spectra for the virgin and stressed sample are shown in Fig. 7 for two parameter sets:

- Set 1: $T_w = 400$ µs, $t_p = 200$ µs, $U_R = -10$ V, $U_P = -0.05$ V.
- Set 2: $T_w = 200$ µs, $t_p = 200$ µs, $U_R = -1.5$ V, $U_P = -0.05$ V.

One can clearly see a significant increase of DLTS signal for the stressed sample, indicating the presence of a full set of different traps. Because of the high




(a) (b)

**Fig. 7:** (a) Obtained DLTS spectra of the virgin and stressed sample with simulated positions of dominant trap peaks. (b) Arrhenius plot of the DLTS spectra measured on the stressed sample for parametric set 2.

complexity of DLTS spectra and the non-exponential character of many transients during measurements, we were able to determine only a few deep levels, mostly metals and corresponding vacancies, which were in perfect congruence with results from the literature.

A direct evaluation method was used for this evaluation. The parameters and position of each trap in spectra was verified by simulation. Results of simulations are also shown in Fig. 7. Parameters and possible origin of each trap are in Tab. 1. Traps that we were not able to verify by simulation are not listed. Based on the character of observed traps, we assume that most of the defects are not generated by HCI, but rather that they are electrically activated. Only trap $T1$ - Oxygen vacancy can be attributed to the degradation of $SiO_2$/Si interface due to HC bombardment.

**Tab. 1:** Parameters of dominant traps.

| Trap # | Possible origin [24] and [25] | $E_t$–$E_V$ (eV) | Sigma ($cm^2$) |
|---|---|---|---|
| $T1$ | O-Vac | 0.180 | $3.00 \cdot 10^{-14}$ |
| $T2$ | Metal impurities in $SiO_2$ | 0.293 | $9.48 \cdot 10^{-14}$ |
| $T3$ | Au-Vac | 0.320 | $2.00 \cdot 10^{-15}$ |
| $T4$ | Metal impurities in $SiO_2$ | 0.365 | $1.73 \cdot 10^{-14}$ |
| $T5$ | Metal impurities in $SiO_2$ | 0.489 | $1.68 \cdot 10^{-14}$ |
| $T6$ | Metal impurities in $SiO_2$ | 0.389 | $1.46 \cdot 10^{-14}$ |
| $T7$ | Au | 0.526 | $1.12 \cdot 10^{-14}$ |

## 4. Conclusion

The influence of repetitive avalanche stress on the electrical performance of DMOS and two types of TrenchMOS transistors has been studied using custom-built UIS test equipment. Degradation of drain-gate capacitance $C_{DG}$ and input capacitance $C_{in}$ was observed in all three types of analyzed structures. However, significant degradation (shift) of $I$–$V$ curves was observed only in Trench MOS devices. DLTS measurements also confirmed the degradation influence of repetitive avalanche stress on the defect distribution.

From the performed analysis, it can be argued that DMOS transistors are less vulnerable to HCI in case of repetitive avalanching than Trench MOS devices. Moreover, we observed that the breakdown voltage in modern middle and high voltage Trench MOS devices is more affected by the repetitive avalanching than in standard low voltage TrenchMOS devices. Using DLTS, several deep levels were observed on stressed samples corresponding to vacancies generated on $Si/SiO_2$ interface and metal impurities originating from the manufacturing process.

## Acknowledgment

This work comes from the European cooperative project R3-PowerUP, which is partially funded by the ECSEL Joint Undertaking under grant agreement no. 737417. This work was also supported by the Slovak Research and Development Agency under contract no. APVV-20-0266 and by Grant VEGA 1/0727/19 supported by Ministry of Education, Science, Research and Sport of Slovak Republic.

## Author Contributions

J.M. and J.K. performed measurements, sample characterization, and processed the data. J.M. and M.M devised the concept, form, and specifications of the UIS tester. J.K. and M.M. contributed to the hardware schematic design, layout, component selection, and programming. A.C. performed simulations and modeling of devices and contributed to a better explanation of results. J.M and L.S performed DLTS measurements. L.S. evaluated DLTS measurements. J.M. and A.C. acquired funding and supervised the project. J.M. wrote the manuscript in consultation with all authors.

## References


[1] WILLIAMS, R. K., M. N. DARWISH, R. A. BLANCHARD, R. SIEMIENIEC, P. RUTTER and Y. KAWAGUCHI. The Trench Power MOSFET: Part I—History, Technology, and Prospects. *IEEE Transactions on Electron Devices*. 2017, vol. 64, iss. 3, pp. 674–691. ISSN 1557-9646. DOI: 10.1109/TED.2017.2653239.

[2] HUARD, V., M. DENAIS and C. PARTHASARATHY. NBTI degradation: From physical mechanisms to modelling. *Microelectronics Reliability*. 2006, vol. 46, iss. 1, pp. 1–23. ISSN 0026-2714. DOI: 10.1016/j.microrel.2005.02.001.

[3] TONG, X., S. LIU, W. SUN, J. WU, Z. YANG, Y. ZHU and L. NI. New Failure Mechanism Induced by Current Limit for Superjunction MOSFET Under Single-Pulse UIS Stress. *IEEE Transactions on Electron Devices*. 2021, vol. 68, iss. 7, pp. 3483–3489. ISSN 1557-9646. DOI: 10.1109/TED.2021.3078718.

[4] SAGARA, M., K. WADA and S.-I. NISHIZAWA. Evaluation of SiC-MOSFET by Repetitive UIS Tests for Solid State Circuit Breaker. *Materials Science Forum*. 2020, vol. 1004, iss. 1, pp. 1010–1015. ISSN 1662-9752. DOI: 10.4028/www.scientific.net/MSF.1004.1010.

[5] CHEN, J. F., K.-S. TIAN, S.-Y. CHEN, K.-M. WU and C. M. LIU. On-Resistance Degradation Induced by Hot-Carrier Injection in LDMOS Transistors With STI in the Drift Region. *IEEE Electron Device Letters*. 2008, vol. 29, iss. 9, pp. 1071–1073. ISSN 1558-0563. DOI: 10.1109/LED.2008.2001969.

[6] NIDHI, K., J.-H. LEE, S.-C. HUANG and M.-D. KER. Energy Transformation Between the Inductor and the Power Transistor for the Unclamped Inductive Switching (UIS) Test. *IEEE Transactions on Device and Materials Reliability*. 2020, vol. 20, iss. 2, pp. 413–419. ISSN 1558-2574. DOI: 10.1109/TDMR.2020.2985306.

[7] RUTTER, P., K. HEPPENSTALL, A. KOH, G. PETKOS and G. BLONDEL. High current repetitive avalanche of low voltage trench power MOSFETs. In: *2009 21st International Symposium on Power Semiconductor Devices & IC's*. Barcelona: IEEE, 2009, pp. 112–115. ISBN 978-1-4244-3525-8. DOI: 10.1109/ISPSD.2009.5158014.

[8] DONOVAL, D., A. VRBICKY, J. MAREK, A. CHVALA and P. BENO. Evaluation of the ruggedness of power DMOS transistor from electro-thermal simulation of UIS behaviour. *Solid-State Electronics*. 2008, vol. 52, iss. 6, pp. 892–898. ISSN 0038-1101. DOI: 10.1016/j.sse.2007.12.006.

[9] PATMANIDIS, K., M. GLAVANOVICS and A. MUETZE. Scalable Multitasking Dynamic Pulse Based Reliability Stress Test for High Voltage Discrete Semiconductors. In: *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*. Ghent: IEEE, 2021, pp. 1–10. ISBN 978-90-75815-37-5.

[10] DIERBERGER, K. Understanding the difference between standard MOSFETs and avalanche energy rated MOSFETs. In: *Studylib* [online]. 2003, Available at: `https://studylib.net/doc/18101057`.

[11] RUTTER, P. and S. T. PEAKE. Low voltage superjunction power MOSFET: An application optimized technology. In: *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. Fort Worth: IEEE, 2011, pp. 491–497. ISBN 978-1-4244-8084-5. DOI: 10.1109/APEC.2011.5744642.

[12] KOH, A. Power MOSFET Single and Repetitive Avalanche Ruggedness Rating. In: *assets.nexperia: Application note* [online]. 2003, Available at: `https://assets.nexperia.com/documents/application-note/AN10273.pdf`.

[13] NIDHI, K., M.-D. KER, J.-H. LEE and S.-C. HUANG. Avalanche Ruggedness Capability and Improvement of 5-V n-Channel Large-Array MOSFET in BCD Process. *IEEE Transactions on Electron Devices*. 2019, vol. 66, iss. 7, pp. 3040–3048. ISSN 1557-9646. DOI: 10.1109/TED.2019.2916032.

[14] KACHI, T., K. EIKYU and T. SAITO. Full-chip simulation analysis of power MOSFET's during unclamped inductive switching with physics-base device models. In: *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. Shanghai: IEEE, 2019, pp. 371–374. ISBN 978-1-72810-581-9. DOI: 10.1109/ISPSD.2019.8757577.

[15] SCHLEISSER, D., D. AHLERS, M. EICHER and M. PURSCHEL. Repetitive avalanche of automotive MOSFETs. In: *2013 15th European Conference on Power Electronics and Applications (EPE)*. Lille: IEEE, 2013, pp. 1–7. ISBN 978-1-4799-0116-6. DOI: 10.1109/EPE.2013.6631934.

[16] ALATISE, O., I. KENNEDY, G. PETKOS, K. HEPPENSTALL, K. KHAN, J. PARKIN, A. KOH and P. RUTTER. Repetitive avalanche

cycling of low-voltage power trench n-MOSFETs. In: *2010 Proceedings of the European Solid State Device Research Conference*. Sevilla: IEEE, 2010, pp. 273–276. ISBN 978-1-4244-6661-0. DOI: 10.1109/ESSDERC.2010.5618365.

[17] KASHYAP, A. S., A. GENDRON-HANSEN, D. SDRULLA, B. ODEKIRK, D. MEYER, C. HONG and W. BROWER. Beyond the Datasheet: Commercialization of 700 V - 1.7 kV SiC Devices with Exceptional Ruggedness for Automotive & Industrial Applications. In: *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. Nuremberg: IEEE, 2018, pp. 1–7. ISBN 978-3-8007-4646-0.

[18] ALATISE, O., I. KENNEDY, G. PETKOS, K. HEPPENSTALL, K. KHAN, J. PARKIN, A. KOH and P. RUTTER. The Impact of Repetitive Unclamped Inductive Switching on the Electrical Parameters of Low-Voltage Trench Power nMOSFETs. *IEEE Transactions on Electron Devices*. 2010, vol. 57, iss. 7, pp. 1651–1658. ISSN 1557-9646. DOI: 10.1109/TED.2010.2049062.

[19] DOYLE, B. S., M. BOURCERIE, C. BERGONZONI, R. BENECCHI, A. BRAVIS, K. R. MISTRY and A. BOUDOU. The generation and characterization of electron and hole traps created by hole injection during low gate voltage hot-carrier stressing of n-MOS transistors. *IEEE Transactions on Electron Devices*. 1990, vol. 37, iss. 8, pp. 1869–1876. ISSN 1557-9646. DOI: 10.1109/16.57138.

[20] LIU, S., R. YE, W. SUN, C. ZHANG, J. WEI, W. SU, A. ZHANG and S. MA. Electrical Parameters Degradations and Optimizations of SOI-LIGBT Under Repetitive Unclamped-Inductive-Switching Conditions. *IEEE Transactions on Electron Devices*. 2016, vol. 63, iss. 4, pp. 1644–1649. ISSN 1557-9646. DOI: 10.1109/TED.2016.2535220.

[21] ALATISE, O., I. KENNEDY, G. PETKOS and A. KOH. Reliability of Repetitively Avalanched Wire-Bonded Low-Voltage Discrete Power Trench n-MOSFETs. *IEEE Transactions on Device and Materials Reliability*. 2011, vol. 11, iss. 1, pp. 157–163. ISSN 1558-2574. DOI: 10.1109/TDMR.2010.2102026.

[22] BERNOUX, B., R. ESCOFFIER, P. JALBAUD and J. M. DORKEL. Source electrode evolution of a low voltage power MOSFET under avalanche cycling. *Microelectronics Reliability*. 2009, vol. 49, iss. 9–11, pp. 1341–1345. ISSN 0026-2714. DOI: 10.1016/j.microrel.2009.06.035.

[23] ZHANG, S., Y. HAN, K. DING, J. HU, B. ZHANG, W. ZHANG and H. WU. Off-state avalanche-breakdown-induced on-resistance degradation in SGO–NLDMOS. *Solid-State Electronics*. 2013, vol. 81, iss. 1, pp. 27–31. ISSN 0038-1101. DOI: 10.1016/j.sse.2012.12.012.

[24] GRAFF, K. *Metal Impurities in Silicon-Device Fabrication*. 1st ed. Berlin: Springer Berlin Heidelberg, 1995. ISBN 978-3-642-97593-6.

[25] CHEN, J.-W. and A. G. MILNES. Energy Levels in Silicon. *Annual Review of Materials Science*. 1980, vol. 10, iss. 1, pp. 157–228. ISSN 0084-6600. DOI: 10.1146/annurev.ms.10.080180.001105.

## About Authors

**Juraj MAREK** received the M.Sc. and Ph.D. degrees in microelectronics from the Slovak University of Technology in Bratislava (STUBA), Bratislava, Slovak Republic, in 2007 and 2011, respectively. He has been a researcher with the Institute of Electronics and Photonics, STUBA, since 2006 and assistant professor from 2020 respectively. His current research interests include modern power devices characterization, reliability, TCAD modeling and simulation.

**Jozef KOZARIK** received his M.Sc. degree in electronics from the Slovak University of Technology in Bratislava (STUBA), Bratislava, Slovak Republic, in 2017. He is currently pursuing his Ph.D. degree at the STUBA Institute of Electronics and Photonics. His research is focused on reliability testing and degradation analysis of wide bandgap semiconductor devices.

**Ales CHVALA** received his M.Sc. and Ph.D. degrees in electronics from the Slovak University of Technology in Bratislava (STUBA), Bratislava, Slovak Republic, in 2005 and 2009, respectively. has been a Researcher with the Institute of Electronics and Photonics, STUBA, since 2007. His current research interests include the TCAD and Simulation Program with Integrated Circuit Emphasis (SPICE) electrothermal modeling, simulation, and characterization of Si, SiC, and GaN based devices.

**Michal MINARIK** received the M.Sc. degree in electronics from the Slovak University of Technology in Bratislava (STUBA), Bratislava, Slovak Republic, in 2020, where he is currently pursuing the Ph.D. degree with the Institute of Electronics

and Photonics. His current research interests include in circuit utilization of Wide-Bandgap (WBG) devices.

**Lubica STUCHLIKOVA** graduated from the Faculty of Electrical Engineering, the Slovak University of Technology (STUBA) in Bratislava, Slovak Republic, in 1990 and received the Ph.D. degree in 1996. She works as a professor at the Institute of Electronics and Photonics, STUBA. Since 1990, she has been interested in semiconductor defects engineering and electrical characterization of semiconductor structures, devices, and materials. Since 2009, her main priority is the investigation of emission and capture processes in GaN-based structures.